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Multiplier Design using Machine Learning Alogorithms for Energy Efficiency

Jane Juma[1], R.M. Mdodo[2], David Gichoya[3]

[1-3]Department of computing and information technology, kenyatta university, Nairobi, Kenya

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Abstract

Designers primary goal is to develop the Adder cell with improved performance viz. speed, fixed rise and fall time, as it the fundamental block in VLSI design process. The dynamic logic circuits are far better than the static logic circuits because it consumes less power and speed performance also increased. But, cascading of several blocks in dynamic logic is found to be a wrong analysis. This drawback of increased complexity with mismatched cascading is overcome by using domino logic circuits. By using domino logic circuits, the reduction of noise margins and increase the speed performance of the circuit is achieved. In this paper, domino logic based Manchester carry chain adder (MCC) is designed using FinFET 18nm technology in Cadence virtuoso. It is noticed that 4-bit and an 8-bit Manchester Carry Chain Adder (MCC) using domino logic design consumes less power and reduction in the delay of the proposed circuit compared with the previous architecture. Implementation results reveal that the 4-Bit MCC Adder has delay of 79.45% less compared to the existed standard design and power consumption also reduced to 94.15%.

Author's e-mail: jene.juma.j@gmail.com, mdodo.rm@gmail.com, david.gich@gmail.com

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Introduction

MCC Adder mainly work on *propagate* and *generate* signals. MCC uses *carry generate* and *carry propagate* signal to determine the carry for every stage. This *carry generate* and *carry propagate* signals are calculated in advance.[1-8] MCC requires a redundant stage to give input carry and also an input clock signal. In ripple-carry adder (RCA) architectures, the generated carry in first stage is passed to the next stage and up to N-stages.[9-14] The overall path delay of RCA is expressed mathematically as follows:

$$t_{delay} = t_{sum} + (N-1)t_{carry} \quad (1)$$

Where t_{carry} and t_{sum} are related to the propagation delays of sum and carry output from first stage to N-stages where N is the total number of stages of the adder module design. From the above equation (1), the majority of total delay of an adder circuit is contributed by t_{carry}. Thus, there is a need to reduce the delay belong to the carry generation path.[15-17] MCA optimizes the propagation delay related to carry path t_{carry}. Therefore, this carry chain improve the speed performance of the addition process of the overall adder block involved.[18-27] The functional verification of the adder blocks is validated with the following Table 1.

Table 1: Characteristic Table

Cin	*B*	*A*	*Sum*	*Cout*	*Carry status*
1	1	1	1	1	Generate
0	1	1	0	1	Generate
1	0	1	0	1	Propagate
0	0	1	1	0	Propagate
1	1	0	0	1	Propagate
0	1	0	1	0	Propagate
1	0	0	1	0	Delete
0	0	0	0	0	Delete

The existing system of MCC adder is designed using CMOS at 180nm technology. The entire circuit design and simulation were done using cadence Tool. The existing MCC adder was designed using dynamic logic circuits. When the dynamic logic MCC adder is compared with the conventional logic circuit, the delay of the circuits is reduced but the power consumption was increased. The major drawback of the existing circuits is power consumption. The channel length is also large.[28-31]

The proposed system of 8-bit MCC adder is designed using FinFET at 18nm technology. The entire circuit design and simulation were done using cadence tool. The proposed circuit has many advantages like suppressed short channel effect, very less channel length, the delay of the circuit is optimized and power consumption is also reduced compared with the previous design.[32-39]

This paper is organized as follows; Section II describes the literature survey on FinFET transistors structural features followed by section III, which discuss about the proposed MCC Adder models. Section IV presents the cadence-based simulation results and their analysis. Section V elaborates the experimental findings of FinFET based MCC Adder. Section VI gives the conclusion of the paper including features and limitations followed by references.

Fundamental Design Aspects of FinFET

FinFET is the structural representation for fin shaped field effect transistor. Chenming Hu with support from his teammates has successfully modeled FinFET. The main objective behind the structure is having a thin body, then the gate capacitance is near to the channel .10nm or less than that width thin is the body. These leads to leakage path far away from the gate can effectively control the leakage.[32-35]

Bulk silicon or silicon on insulator (SOI) wafers are used for implementation of FinFET. The substrate consists of a thin fin of silicon body. The three sides of the channel are controlled due to wrapping of gate around the channel. The structure is said to be FinFET since Si body similar to the fish's back fin. The below Fig. 1 represents the 3-D model of FinFET structure.[16]

Bulk MOS has the channel which is horizontal. Where as in FinFET the Channel is vertical. Width of device is Height of the channel (Fin) in the FinFET. Perfect Width of Channel is given by

$$Width\ of\ channel = 2 * Fin\ Height + Fin\ width \quad (2)$$

Increase in the height of the channel fin leads to increase in the width therefore leads to increase in the drive current of FinFET. Parallel construction of multiple fins connected together shown in Fig. 3 also leads to increase in the device drive current. Devices drive strength can be determined by varying channel width seen in Planar devices.[17-19]

Reduction in short channel effects and ensuring high V_t (Threshold) is seen in conventional MOS, where as in FinFET provides better SCE (Short Channel Effect), therefore doping of channel become optional this is due to wrapping of gate structure around the channel and body is thin. The fundamental variation of the MOSFET and FinFET is summarized in the Table 2.

Proposed Adder Models

8-Bit MCC Adder

The 8-bit MCC Adder is applicable to optimize the delay and to increase the speed of the circuit. The 8-bit MCC Adder is mainly used instead of 4-bit MCC Adder as a building block, can lead to most efficient and high-speed adder implementation. The 8-bit MCC Adder consists of two 8-bit inputs namely P_7,

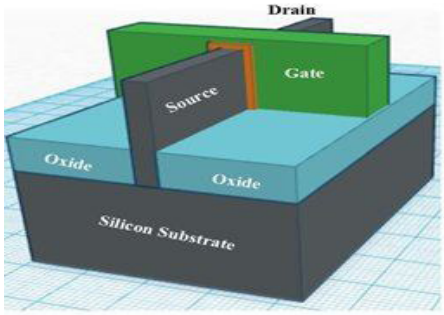

Fig. 1: 3-D model of FinFET structure

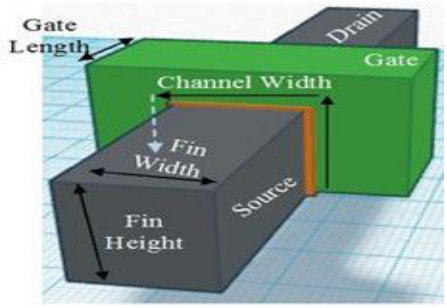

Fig. 2: Planar model of FinFET Structure.

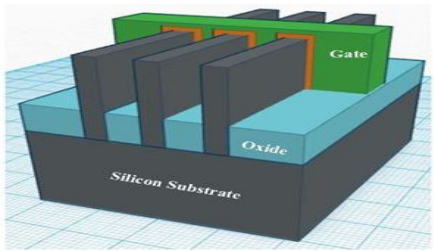

Fig. 3: Multi-Fin structure.

Table 2: Comparision Table of FinFET and MOSFET

MOSFET	*FinFET*
Lower driven currents	Higher driven currents
High leakage currents	Low leakage currents
Short Channel Effect is present	Suppressed Short Channel Effect (SCE)
It consumes more power	It consumes less power
Scaling and Mobility of transistor is not applicable for less than 40nm	Scaling and Mobility of transistor is applicable less than 28nm

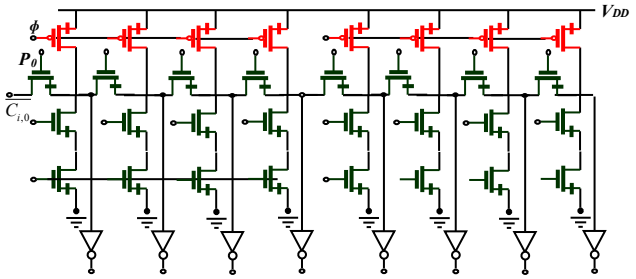

Fig. 4: 8-bit MCC Adder

P_6, P_5, P_4, P_3, P_2, P_1, P_0 and G_7, G_6, G_5, G_4, G_3, G_2, G_1, G_0. The clock signal is used control the entire operation of the circuit. The input values are getting from G_i and P_i of the *carry generate* and *carry propagate* signal. If CLK value is equal to logic '0' or LOW, then the circuit will be in the pre-charge state and it holds logic '0' for every output. If CLK value is change from LOW to HIGH then the output values will depends on the inputs. The inputs *carry generate* and *carry propagate* signal outputs from G_i and P_i and the corresponding carry output signals are C_7, C_6, C_5, C_4, C_3, C_2, C_1, C_0. The above Fig. 4 represents the 8-Bit MCC Adder [20]-[21].

The operation of 8-bit MCC Adder is same as the 4-bit MCC. The inputs of every stage Pi and Gi are

$P_7 = A_7 \oplus B_7$ $\quad G_7 = A_7.B_7$
$P_6 = A_6 \oplus B_6$ $\quad G_6 = A_6.B_6$
$P_5 = A_5 \oplus B_5$ $\quad G_5 = A_5.B_5$
$P_4 = A_4 \oplus B_4$ $\quad G_4 = A_4.B_4$
$P_3 = A_3 \oplus B_3$ $\quad G_3 = A_3.B_3$
$P_2 = A_2 \oplus B_2$ $\quad G_2 = A_2.B_2$
$P_1 = A_1 \oplus B_1$ $\quad G_1 = A_1.B_1$
$P_0 = A_0 \oplus B_0$ $\quad G_0 = A_0.B_0$

4-Bit MCC Adder

The Fig. 5 represents the 4-bit MCC Adder. It mainly has two 4-bit inputs namely G_3, G_2, G_1, G_0 and P_3, P_2, P_1, P_0. For every stage, the inputs are getting from *carry propagate* and *carry generate* signal outputs. The clock signal controls the operation of the circuit. If clock signal equals to LOW or logic '0' then the circuit is in the pre-charge state and it holds logic '0' for every output. If clock value is change

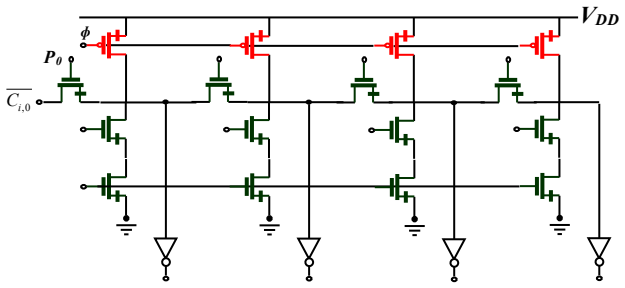

Fig. 5: 4-bit MCC Adder

from logic '0' to logic '1', then the output is depends on the inputs. The *carry propagate* and *carry generate* inputs from first stage to fourth stage will possesses and corresponding carry outputs are generated namely C_3, C_2, C_1, C_0.

In the figure 5, initial inputs are A, B and C_{in}. C_{in} must be always either logic '0' or logic '1' for the MCC. The inputs of P_i and G_i for every stage are

$P_3=A_3 \oplus B_3$ $\quad G_3=A_3.B_3$
$P_2=A_2 \oplus B_2$ $\quad G_2=A_2.B_2$
$P_1=A_1 \oplus B_1$ $\quad G_1=A_1.B_1$
$P_0=A_0 \oplus B_0$ $\quad G_0=A_0.B_0$

Case 1: When A=0 and B=0

If Clk=1, P=A⊕B=0 and G=A.B=0 then Cout =0.

In this case the output of P, G and Cout is always be logic '0'.

Case 2: When A=1 and B=0

If Clk=1, P=A⊕B=1 and G=A.B=0

In this case the propagation P output is equal to '1' then $C_{out}=C_{in}$ i.e., the input of carry is straightly moving to the output of carry. The circuit is in carry propagation state.

Case 3: When A=1 and B=0

If Clk=1, P=A⊕B=1 and G=A.B=0

In this case the propagation P output is equal to '1' then C_{out}=Cin i.e., the input of carry is straightly moving to the output of carry. The circuit is in carry propagation state.

Case 4: When A=1 and B=1

If Clk=1, P=A⊕B=0 and G=A.B=1

In this case the generation G output is equal to '1' then C_{out}=1. The circuit is in carry generation state.

In all the above cases, when Clk='0' the carry output C_{out}=0. The same analogy is applicable for both 8-bit and 4-bit MCC adders.

Outcomes of the Standard Models

4-Bit MCC Adder

The MCC adder of 4-bit capacity is designed using FinFET nodes and the same has presented in the Fig. 6. The required configurations corresponding to inverter modules

V_{DD}

ϕ

too has designed using the same FinFET models. Similarly, the propagation and generation signal symbol are created which has multiple number of n-LVT and p-LVT.

Transient response of 4-Bit MCC adder

The response of a system to a change from a steady state or equilibrium state is known as Transient response. The transient is not definitely tied to *on* or *off* state, but to any state that affects the steady state of the system.

The schematic diagrams or circuit design of 4-bit and 8-bit MCC Adder are simulated using Cadence software and FinFET 18nm technology to obtain transient response.

From the transient response figures, 0V represents logic '0' which implies 'OFF' state and where as 1V represents logic '1' which implies 'ON' state.

In FinFET, the maximum voltage is considered up to 1V. This means that V_{DD} is 1V and GND is 0V. FinFET cannot withstand high voltages that are greater than 1V as it leads to the damage of transistors.

The Fig. 7 represents the transient response of 4-bit MCC Adder. The entire simulation is done using Cadence virtuoso at FinFET 18nm technology.

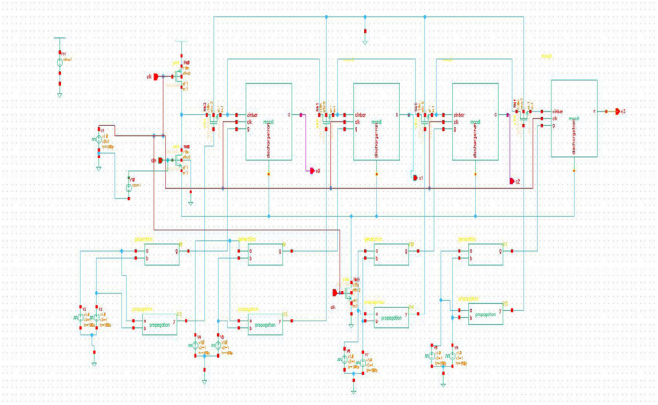

Fig. 6: Schematic diagram of 4-bit MCC Adder.

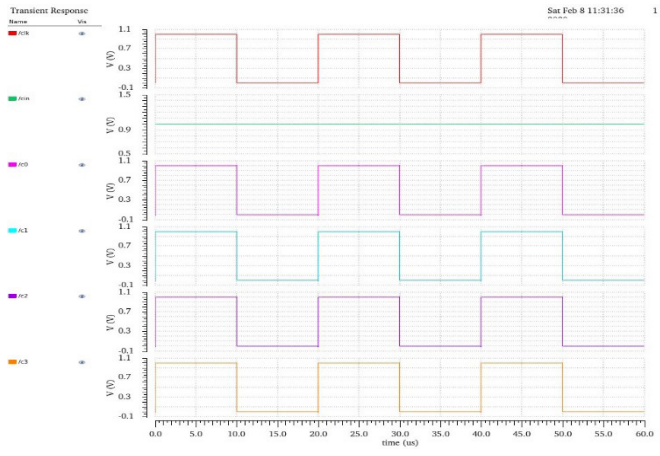

Fig. 7: Transient response of 4-bit MCC Adder.

Experimental Findings

Using Cadence virtuoso FinFET 18nm spectre models, the following outcomes for 4-bit MCC Adders are observed.

Delay Metric

It is observed from the above delay analysis Table 3, the propagation delay of the proposed design has the considerable impact of delay reduction. The proposed design has reduced delay value of 0.1013ns. When compared with previous design of 4-bit MCC Adder, the proposed model has reduced delay of about 80% less.

Power Metric

From the Table 4, the power consumption of the proposed circuit is also reduced. The proposed design has reduced power consumption value of 1.005uW. When compared with previous standard design, the energy dissipation for the design of the circuit shown in Fig. 6 is reduced by 94.15%.

The PDP values presented in the above Table V shows the reduction of the PDP metric compare to that of previous standard models. PDP for the design of Fig. 6 is reduced by 98.79% to the original conventional MOS transistor version.

It can be noticed from the above EDP analysis Table VI, hence from previous delay and PDP measures too, even EDP also has the proportionate minimized value. When compared with previous standard design, the EDP for the design of Fig. 6 is reduced by 99.75%.

Table 3: Delay Analysis Table for 4-bit MCC Adder

Existing design (4-Bit MCC Adder)	*Proposed design (4-Bit MCC Adder)*	*Change in delay (%)*
0.493ns	0.1013ns	79.45% Decrease

Table 4: Power Analysis Table for 4-bit MCC Adder

Existing design (4-Bit MCC Adder)	*Proposed design (4-Bit MCC Adder)*	*Change in delay (%)*
17.18uW	1.005uW	94.15% Decrease

Table 5: PDP Analysis Table for 4-bit MCC Adder

Existing design (4-Bit MCC Adder)	Proposed design (4-Bit MCC Adder)	Change in PDP (%)
8.47*10-15J	1.02*10-16J	98.79% Decrease

Table 6: EDP Analysis Table for 4-bit MCC Adder

Existing design (4-Bit MCC Adder)	Proposed design (4-Bit MCC Adder)	Change in EDP (%)
4.175*10-24Js	1.033*10-26Js	99.75% Decrease

Conclusion

Cadence virtuoso is used to design and simulate the MCC circuits. There is an excellent improvement in reduction of the power consumption and delay of the proposed circuit and the performance and speed of the circuit is increased. The performance is analysed by using 18nm FinFET spectre models. The simulation results demonstrates reduced power consumption and delay values of 4-bit and 8-bit MCC Adders. The reduced power and delay values of 4-bit MCC adder are 1.005uW and 0.1013ns, respectively. When compared with previous design of 4-bit MCC Adder, the delay of the proposed FinFET based circuit reduced by 79.45%. It also observed that the power consumption of 4-bit MCC Adder compared with previous design is reduced by 94.15%. Hence, the proposed 4-bit and 8-bit MCC Adders are highly efficient compared with the previous design. As a further work minimization of the distortions through various combinations of logics and designing the MCC adders for complex circuits or higher variables like 16, 32, 64 bit can be done. The paper further extended by reducing the channel length or designing in submicron technology and decreasing the area of this chain.

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