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Research Article

ESTIMATION OF RELIABILITY OF D FLIP-FLOPS USING MC ANALYSIS

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ABSTRACT
As the day by day size of the electronic devices has been decreased by scaling down the of the VLSI technology. For any electronic devices reliability is one of the best performance indicator which decides the life time of the any device. In this paper we investigated the performance of thelow power edge triggered d flip flop and dual edge triggered static pulsed flip-flop respectively. Simulated the given circuit in cadence virtuoso environment using the 180 nm technology. To estimate the reliability we used the Monte Carlo analysis and applied at different corners such as SS,SF,FS,FF and TT respectively.
Keywords: D-Flip-Flops, Monte Carlo analysis, cadence virtuoso

INTRODUCTION

The current fourth industrial revaluation electronic devices plays prominent role in our day to day life. Devices like laptops, cell phones, and many electronic devices are to be operated in high speed and low power. Therefore, to reduce the power consumption operation of the circuits in a sub threshold region is one of the biggest challenge in present day scenario in VLSI technology. At present digital world flip-flops becomes one the crucial and most important circuits in many portable devices like phase detectors, memories, security devices, microprocessors and many other applications[1-5].Any electronic devices at present day scenario it consumes the almost 40-80% of total power in any system. As along the technology is rampant growth the latency of the circuit is going to be reduced. The reduction in power is results greatly impact the speed of the circuit respectively. Power consumption of the any circuit can be given by equation 1.

$$P_d=\alpha C_L V_{dd}^2 f_{clk}+ V_{dd}I_{sc} + V_{dd}(I_{leakage} + I_{static}) \quad (1)$$

From the above equation Pd=power dissipation,CL= load capacitance,I_{sc}=short circuit current, F_{clk}=clock frequency, $I_{staitic}$=static power respectively. The power consumption of the any electronic device can be classified in to three categories such as static power, dynamic power and switching power.there are a wide verity of flip-flops has been studied in the literature survey to reduce the power dissipation and improve the performance of the VLSI. There several approaches have been discussed to assess the metrics of the D flip flops[5-8]. In this paper we analysing the impact of the ageing and reliability of the D- flip flops using the Gaussian distribution techniques. The rest of the paper is organised as follows such as section 2 describes the literature survey of the different types of flip-flops and section 3 describes the reliability of the different flip flops using 6 sigma analysis respectively.

Literature Survey

Dual Edge Triggered Static Pulsed Flip-Flop(Detspff)

the schematic of the DETSPP as shown in figure 1.it consists of total four inverters which are used to generate the delayed and inverted outputs. The obtained signals from pulse generator and along with two NMOS pass transistors generates the a narrow sampling window in two edges such as rising and falling edges respectively.

Whenever the pulse signal being applied to the CMOS D flip flop as a results both N1 and N2 transistors being switched to ON and pass the data through SB and Rb respectively. Because of symmetric sizes of the all the transistors it produces the equal rise and fall times respectively. Therefore it produces the high voltage drop and high leakage current[9-11].

Low Power Edge Triggerd D Flip Flop(Lpedff)

In order to enhance the performance metrics of the D flip flops and reduce the power consumption and delay authors has been proposed a low power edge triggered D flip flop. figure 3. depicts the low power edge triggered D flip flop. The narrow pulse at both the rising and falling edge of the latch are equally distributed the clock. whenever the data is being applied to the D flip flop the data has been transfer to the output the response being inverted to either Q and Qb respectively[12-15].

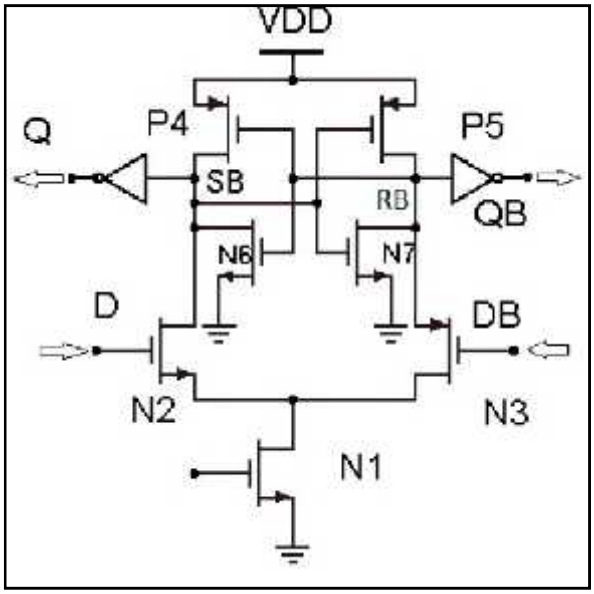

Figure 1: SCHEMATIC OF DETSPFF .

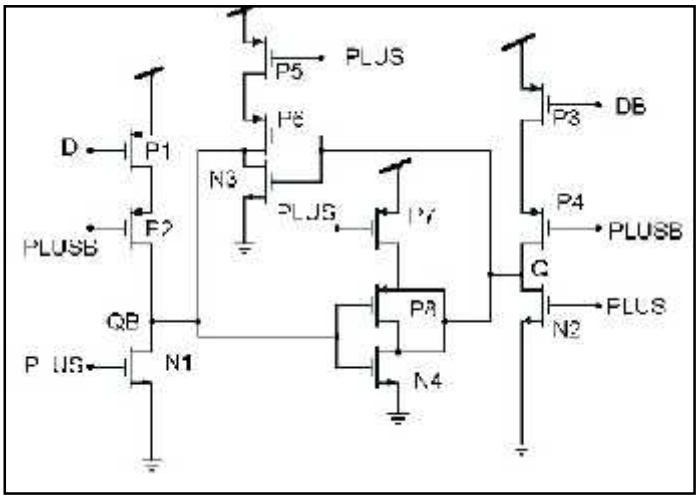

Figure 3: LOW power dual edge triggered flip-flop

Estimation Of Reliability For The Detspff And Lpedff

The circuit operation were simulated using the cadence virtuoso using the 180 nm technology cadence spectre as a simulator. In order to estimate the reliability of the above two flip flops applied a statistical analysis such as Monte carol analysis. we applied the 100 number of samples at each stage respectively. the obtained results from MC analysis as shown in figure 4 and 5 respectively.

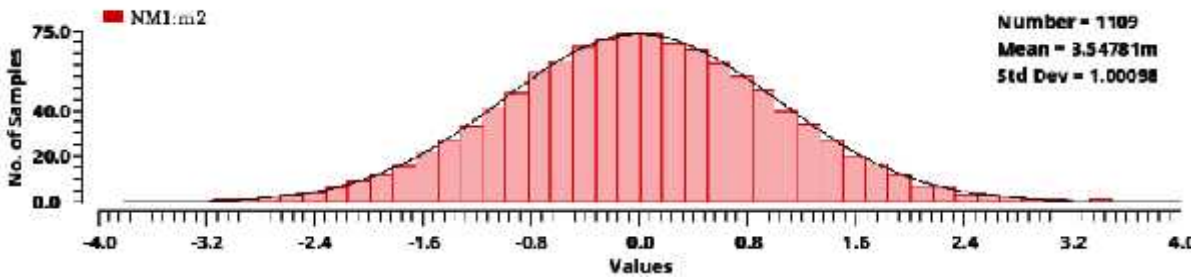

Figure 4: Reliability representation of DETSPFF with respect to histogram

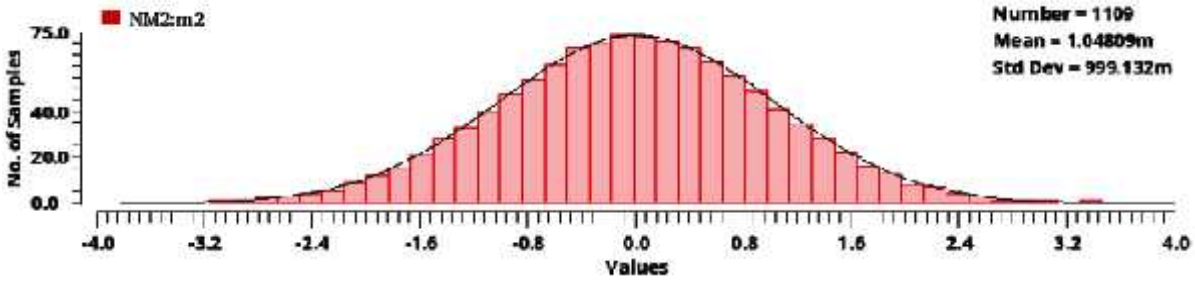

Figure 5: Reliability representation of LPEDFF with respect to histogram

From the above obtained results it clearly indicates the LPEDFF is more reliable as compared to the DETSPFF. As from the dispersion of the samples ratio is comparatively very less which is 1.04809m for the LPEDFF and DETSPFF is 3.5478 respectively.

Table 1:reprasentaion of reliability for both DETFF and LPEDFF

Type of FF	Reliability	No .of samples
DETSPFF	48.99	100
LPEDFF	45.36	100

Conclusion

Reliability is one of the crucial parameter for the any of the digital circuits. Here in this paper we discussed the reliability of the two flips such as DETSPFF and LPEDFF D flip flops respectively. we have verified the reliability at different corners such as SS,SF,FS,FF and TT.

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