Journal of VLSI Circuits and Systems, ISSN: 2582-1458 Vol. 5, No. 1, 2023 (pp. 35-41)

RESEARCH ARTICLE WWW.VLSIJOURNAL.COM

Memory Module: High-Speed Low Latency Data Storing Modules

Doris Klein[1], Stefan Dech[2], Bradley Raddwine[3], Ernst Uken[4]

[1-4]Faculty of Engineering, University of Cape Town (UCT), South Africa

KEYWORDS:
6T SRAM;
Cadence Virtuoso;
MOSFET; Efficiency;
Power consumption;
Standby leakage current.

ARTICLE HISTORY:
Received 06.07.2022
Accepted 14.08.2022
Published 23.09.2022

DOI:
https://doi.org/10.31838/jvcs/05.01.05

Abstract

The electronics devices are facing a foremost drawback of standby leakage, which severely impacting the electronics industry from the past few decades. As well as the need for cache memory is proportionately increasing with the data processing frequency of the processors. SRAM is used for cache reminiscence layout. Many low-energy techniques are considered to minimize the current leakage. Full MOSFET 6T SRAM mobile is the main application used for designing digital circuits. This task implements 6T MOSFET SRAM cell. The usage of FinFET spectra models, the layout, and circuit level software implementations are carried out using FinFET 18nm nodes. The power intake, mainly off-state leakage, present-day, is every other major problem being confronted inside the present-day technology of electronic enterprise because the chip densities increase with a wider variety of transistors. Energy consumption is the fundamental disadvantage in the SRAM model evaluation. Considering the salient features of the FinFET, 6T SRAM cell is designed at 18nm FinFET spectre models, and it is compared in contrast to MOSFET standard cell in support to the simulation results.

Author's e-mail: Klein.doris@engfacuct.ac.za, dech.stefani@engfacuct.ac.za, radd.bradley@engfacuct.ac.za, uken.ern@engfacuct.ac.za

How to cite this article: Klein D, Dech S, Raddwine B, Uken E. Memory Module: High-Speed Low Latency Data Storing Modules. Journal of Complementary Research, Vol. 5, No. 1, 2023 (pp. 35-41).

Introduction

Sub-threshold current due to the low threshold voltage, gate leakage current due to very thin gate oxide and eventually band to band tunneling due to the excessively doped halo doping profile is some of the noted sources responsible for leakage currents in electronic devices. A resonant submicron MOSFET transistor's leakage current consists of three components: the tunneling current of the junction, the sub-threshold current and the tunneling current of the exit.[1-3], [16], [17]

SRAM is a type of RAM. There lie some differences with DRAM. SRAM is designed to meet two basic needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. SRAM is better in terms of speed resulting in faster operation. As a result, it takes less amount of time for accessing data. It is used to create speed sensitive cache and has medium power consumption.[18], [19]

The power consumption of SRAM varies widely depending on how frequently it is accessed. Numerous techniques have been proposed to manage the power consumption of SRAM-based memory structures.[20] SRAM exhibits volatile memory in other words; the memory is lost when power is not supplied. It uses bistable latching circuitry, which is a circuit that has two stable states; in other words, it is a bistable multivibrator.[21] This circuit allows the states to be changed by the inputs that are applied. Based upon the inputs, the respective outputs will be obtained. This bistable circuit's main job is to store the information bit by bit. A bi-stable circuit can have at least four to six transistors in its structure.[22]

SRAM is widely used in electronics devices such as mobile phones, workstations, routers etc. SRAM allows data to be accessed quickly, but it is quite large in size compared to DRAM. As it uses a more significant number of transistors, it is quite expensive.[23]] It is the main job to perform read and write operations. In SRAM the memory is in the form of arrays, i.e. the memory is arranged in rows

and columns that are called as word lines and bit lines. SRAM are also used in portable devices.

A typical SRAM cell is made up of six transistors that form two cross-coupled inverters. When the SRAM is performing, it creates and manipulates the variables. It has low latency and high speed to access data. There are many companies, such as IBM that design SRAM and release it into the market.[24] Before the introduction of FinFET, MOSFET was widely used. MOSFET further had technologies namely GPDK 180nm, 90nm and 45nm. There were significant limitations that are associated with MOSFET such as high propagation delay, high leakage current, high power dissipation and consumption and low operating speed which led to the decline in efficiency and performance. Due to these factors, the MOSFET technology was not acceptable in accordance with the expectations of the electronic industry. To overcome the limitations of MOSFET technology, another technology, namely FinFET has been introduced.[25], [26]

In this paper, we will be discussing the FinFET technology with its advantages and limitations, along with its respective pictorial representation. Later, there will be an in-depth explanation about what SRAM is, along with its importance in the electronic industry. The structure of 6T SRAM cell has been explained from one transistor to another transistor. Its block diagram is given for a better understanding of the structure. Later, there will be an explanation about SRAM operation along with its truth table using FinFET. The resultant truth table obtained is also given. Going further, a schematic will be designed using FinFET technology, and the graphs that have been obtained by using the software will be verified with the respective truth table of the technology. Once the graph is verified with the truth table, we will start observing the transient responses. Apart from the transient responses, we will be observing the power and delay graphs of FinFET. Based upon the power and delay values, a comparison table is drawn.

The Primary Advancements of FinFET Modeling

FinFET in simple terms is a multi-gate. In this type of technology, the MOSFET is fabricated on a substrate, where the gates are placed on different sides of the channel. By this, it forms a double gate structure. FinFET has a three-dimensional type of structure. The persistent increase in the levels of integration has led to the birth of FinFET technology. In continuation with the previous existing technologies, the size of the transistors can be less than 20nm. Because of this feature, FinFET was widely used since 2014. It also overcame the drawbacks that were associated with MOSFET technology.[27-30] Fig. 1 represents the schematic diagram of FinFET in three-dimensional views.

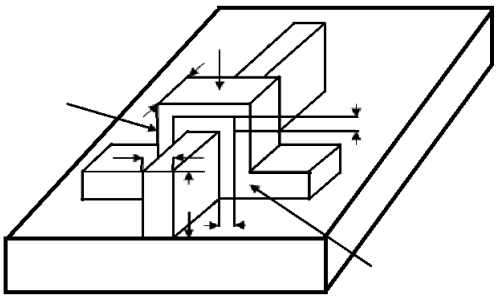

Fig. 1: FinFET Structure

It was also proven that FinFET could be two independent electric gates which give more flexibility with efficiency and lower power gates. One of the many applications of FinFET is the replacement of switches that were primarily built using MOSFET with FinFET. The reason being is that FinFET had better performance when compared to MOSFET. FinFET also provided low leakage current and improved on-off current ratio gives FinFET an upper hand over MOSFET. FinFET is also used in designing modern processors. The advantages of FinFET are that with an increase in voltage for circuits, results in low gate resistance. There are many more advantages of FinFET apart from the ones mentioned above when compared with MOSFET. The propagation delay is less compared to that of MOSFET 180nm and 90nm. It has a higher drive current. The speed is higher. The power consumption also decreases along with power dissipation.[31, 32]

In recent times, the FinFET technology has seen an increase in adoption in integrating circuits. The FinFET technology provides the superior levels of scalability that is needed to ensure the present progress with increased levels of integration. The FinFET technology provides many advantages in terms of IC processing which means that it is adopted as a significant way within the IC technology.[33-43]

Standard SRAM circuit Using MOSFET and FinFET Models

The circuit construction and operation of the 6T SRAM in both MOSFET and FinFET versions with their mode of operation has presented in this section. The representation of the FinFET based transistors is given by their respective colored representation with an extra added fin.

Conventional 6T SRAM cell

The Fig. 2 gives the schematic diagram of conventional 6T SRAM cell designed using gpdk 180 nm technology.

6T SRAM using FinFET

To overcome the limitations that are associated with the MOSFET technique, we have used 18nm FinFET spectre models. The 6T SRAM built using MOSFET technology lower than 45nm has the reliability and parametric issues. The

structure of 6T SRAM using FinFET has shown in Fig. 3. In similar to the Fig. 2, It has two cross-coupled inverters in which it forms a reversal connection by neutralizing inverters to the original values.

The SRAM transistor cell can store one bit at a time. Each time a data must be stored; it will process bit by bit. The output potential of the inverter is given as the input to the other inverter. That is, Q' is the output of transistors M4 and M5. This is then given as the input to transistors M2 and M3. Similarly, Q is the output of transistors M2 and M3. This is then fed as the input for transistors M4 and M5. This can be termed as a feedback loop. This feedback loop tends to stabilize the cross coupled invertors to their respective states.

SRAM has three types of modes: standby mode, write mode and read mode. It is said to be in standby mode when the write line is low, that the input to the write line is given as 0. So, when the write line is 0, the two access transistors N2 and N4 are turned off as the write line is the input to them. When the access transistors are OFF, the two inverters are in complementary with each other. The reason for this is that there is no input being given to the two invertors. When the PMOS transistor of the left inverter is turned ON, the output of the inverter would be high.

This is then given as the input to the right inverter. Since the input is high, the PFinFET transistor of the right inverter turns OFF concerning the FinFET logic and output obtained at the right inverter is low. This is also known as read mode. Now coming to the write mode, the input of the write line is given as high in other words, it is given as 1. By this, the two access transistors turn ON. When the two access transistors turn ON, they act as the inputs to the inverters. The data that needs to be written are fed to the bit line and the inverse data is given to the complementary bit line. As the input to the bit line is one, a path is created from the access transistor to Q'. Upon reaching Q' the voltage decreases to 0.

This is then given as the input to the left inverter. Then PFinFET transistor of the left inverter turns ON, and the NFinFET transistor turns OFF. The output Q is then 1. This is then given as the input to the right inverter, therefore which we would obtain 0 at Q'. This is case is correct as both the outputs are complementing each other. When it comes to read mode, whatever the data is stored previously, that data will be displayed. The operation of 6T SRAM can be verified using the truth table given in table I as it represents the characteristics of the SRAM cell.

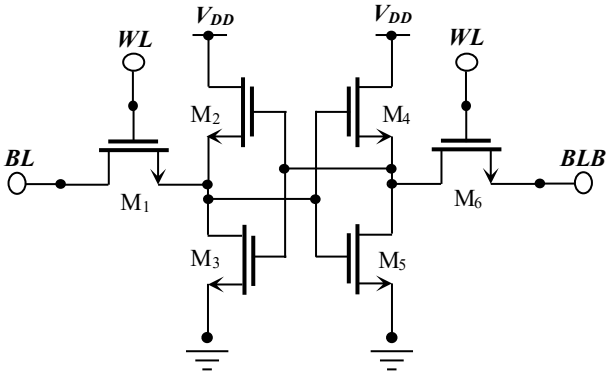

Fig. 2: MOSFET based 6T SRAM circuit diagram

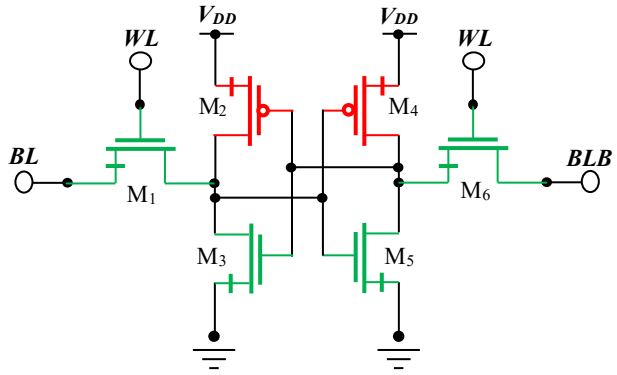

Fig. 3: FinFET based 6T SRAM circuit diagram

Table 1: SRAM Truth Table

WL	*Bit line*	*Bit line bar*	*Q'*	*Q*
1	1	0	0	1
0	1	0	0	1
1	0	1	1	0
0	0	1	1	1

Cadence Based Design Modelling and Performance evaluation

FinFET Simulation

The spectre models of 18nm FinFET is considered for developing the SRAM modules in cadence virtuoso.

The design parameters of MOSFET SRAM and FinFET SRAM are shown in Fig. 4 and Fig. 5; and are tabulated in Table 2.

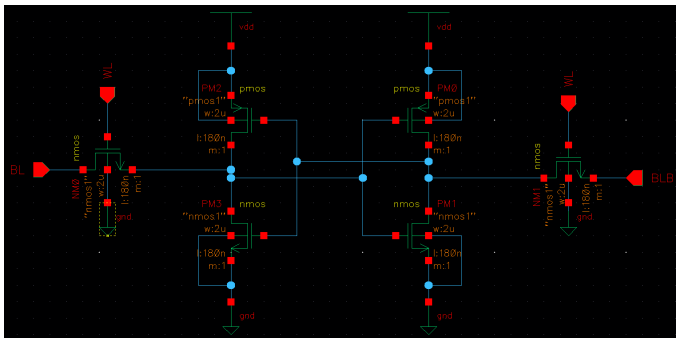

Fig. 4: The 180 nm technology MOSFET based 6T SRAM implementaion of the circuit shown in Fig. 2

Fig. 6 is the transient response of FinFET based SRAM as shown in Fig. 5. The transient response has met all the conditions of SRAM as mentioned in Table I.

Figures 7 and 8 are the power dissipation and propagation delay Vs V_{DD} of 6T SRAM cells. The power supply has varied from 0.1V to 1V and the response has presented in the Fig. 5 and Fig. 6, respectively.

Observing the graphs in Fig. 5 and Fig. 6, we can see that there is an increase in power dissipation when the power supply has increased from 0.1V to 1V, but at the same variation of supply voltage, the decrease in the propagation delay can be observed from the delay Vs VDD graph. When compared the power and delay of all MOSFET 180nm, 90nm, and 45nm with FinFET, we observed that the power and delay are less in FinFET designs than MOSFET designs. But the power and delay should still be in challenging levels to meet the industrial expectations.

Layouts of MOSFET and FinFET based SRAMS

The conventional MOSFET based 6T SRAM has occupied 95um^2 of effective area. The FinFET based 6T SRAM has occupied 1.37um^2 of effective area.

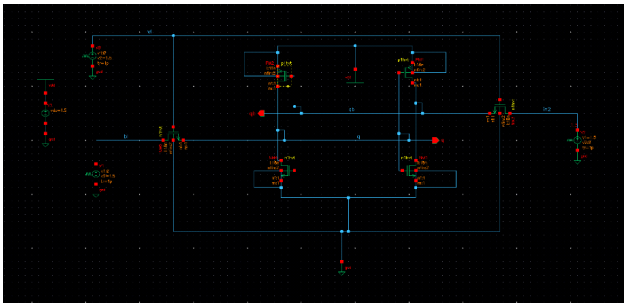

Fig. 5: The 18nm FinFET based 6T SRAM implementaion of the circuit shown in Fig. 3

Table 2: The Transistors Aspect Ratios of the circuits shown in Fig. 4.

	MOSFET based SRAM (Fig. 2)	
Transistor	*W (nm)*	*L (µm)*
M1, M2, M3, M4, M5, M6	180	2

Table 3: The Transistors Aspect Ratios of the circuits shown in Fig. 5.

	FinFET based SRAM (Fig. 3)	
Transistor	*W (nm)*	*L (µm)*
M1, M2, M3, M4, M5, M6	18	0.36

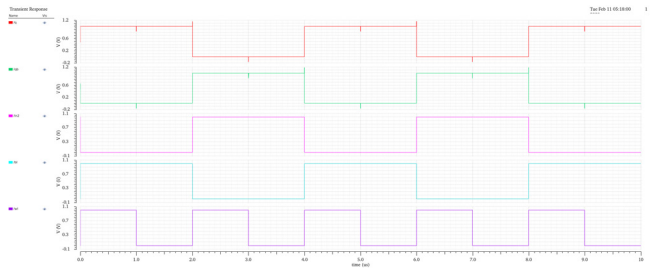

Fig. 6: Transient Response of FinFET

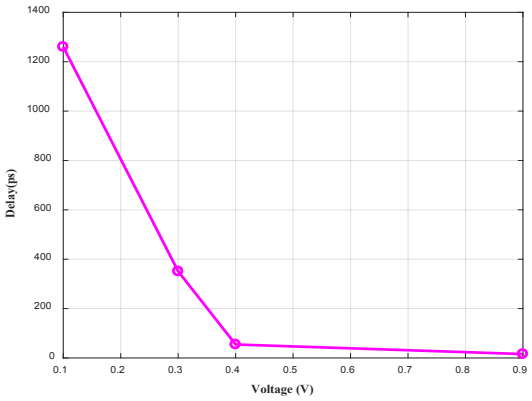

Fig. 7: Propagation delay Vs V_{DD} of FinFET

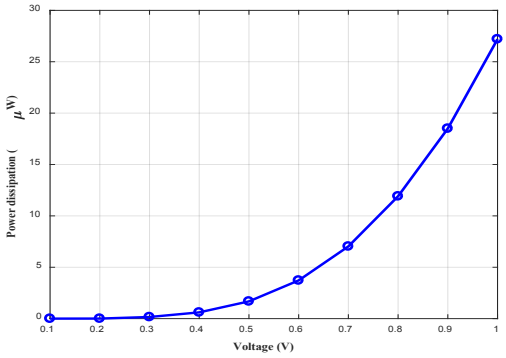

Fig. 8: Variation of Power dissipation Vs V_{DD} of FinFET

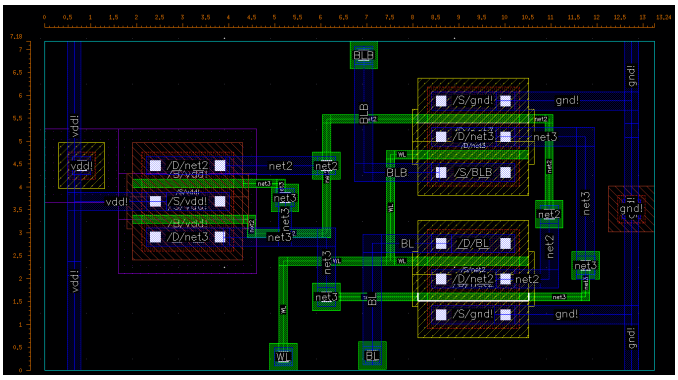

Fig. 9: Layout representation of Fig. 2.

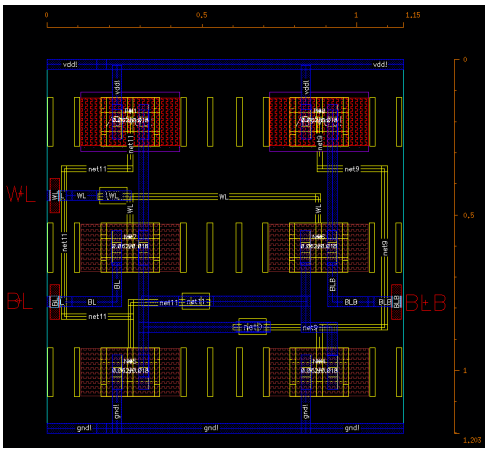

Fig. 10: Layout representation of Fig. 3.

Table 4: Performance Validation of MOSFET and FinFET designs

Technology	*Power*	*Delay*	*PDP*	*EDP*
MOSFET (Fig. 2)	14.2 mW	4.3 ns	61x10-12 J	0.261 x10-18 Js
FinFET (Fig. 3)	16.8 µW	0.4 ns	6.72x10-15 J	2.69 x10-24 Js

Designing a 6T SRAM with less than 45nm is not desirable as MOSFET offers higher gate resistance, which produces the uncontrolled flickering noise. From table II, we can observe that the power and delay values are less for the FinFET technology when compared to MOSFET technology.

Conclusion

In this paper, the vital factors which contribute to the usage of SRAM in the electronic industry have discussed in comparison to the advantages and disadvantages that SRAM possesses. The components that are responsible for current leakage in SRAM has discussed and plotted. Even though MOSFET was initially used more for the higher technologies greater than 45nm, it had some disadvantages which led to decrease in efficiency when MOSFET scaling has made below 28nm technology. In order to meet the limitations caused in MOSFET, FinFET has been introduced and offers significant improvements in the performance metrics. The designed SRAM at 18nm FinFET spectre models has performed with much advantages in comparison to that of MOSFET based conventional design. The simulation results and layouts of the same have concluded the meritorious advantages of the FinFET.

References

[1] "International technical roadmap for semiconductors," 2009 available online at http:// www.itrs. net/links/ 2009ITRS/home2009.htm

[2] S. Sushma, S. Swathi, V. Bindusree, Sri Indrani Kotamraju, A. Ashish Kumar, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "QCA Based Universal Shift Register using 2 to 1 Mux and D flip-flop," IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[3] M. Sreevani, S. Lakshmanachari, B. Manvitha, Y.J.N. Pravalika, T.Praveen,V.Vijay, Rajeev Ratna Vallabhuni, "Design of Carry Select Adder Using Logic Optimization Technique," IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[4] M. Saritha, Chelle Radhika, M. Narendra Reddy, M. lavanya, A. Karthik, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Pipelined Distributive Arithmetic-based FIR Filter Using Carry Save and Ripple Carry Adder," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[5] L. Babitha, U. Somanaidu, CH. Poojitha, K. Niharika, V. Mahesh, and Vallabhuni Vijay, "An Efficient Implementation of Programmable IIR Filter for FPGA," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[6] K. C. Koteswaramma, Ande Shreya, N. Harsha Vardhan, Kantem Tarun, S. China Venkateswarlu, and Vallabhuni Vijay, "ASIC Implementation of division circuit using reversible logic gates applicable in ALUs," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[7] Vallabhuni Vijay, J. Sravana, K.S. Indrani, G. Ajitha, A. Prashanth, K. Nagaraja, K.C. Koteswaramma, C. Radhika, M. Hima Bindu, N. Manjula, "A SYSTEM FOR CONTROLLING POSITIONING ACCORDING TO MOVEMENT OF TERMINAL IN WIRELESS COMMUNICATION BASED ON AI INTERFACE," The Patent Office Journal No. 50/2021, India. Application No. 202141055995 A.

[8] Dr. L.V. Narasimha Prasad, Dr. Vijay Vallabhuni, Dr. S. China Venkateswarlu, Dr. V. Vhandra Jagan Mohan, Ms. P. Sruthilaya, Mr. K. Tarun Kumar, Mr. B. Raju, Mr. P. Ravinder, "Garbage Collector with Smart Segregation and Method of Segregation Thereof," The Patent Office Journal No. 04/2022, India. Application No. 202141062270 A.

[9] Sravana, J., K. S. Indrani, M. Saranya, P. Sai Kiran, C. Reshma, and Vallabhuni Vijay, "Realısatıon of Performance Optımısed 32-Bıt Vedıc Multıplıer," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 14-21.

[10] V. Vijay, J. Prathiba, S. Niranjan Reddy, V. Raghavendra Rao, "Energy efficient CMOS Full-Adder Designed with TSMC 0.18µm Technology," International Conference on Technology and Management (ICTM-2011), Hyderabad, India, June 8-10, 2011, pp. 356-361.

[11] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Optimal design of VLSI implemented Viterbi decoding," National conference on Recent Advances in Communications & Energy Systems, (RACES-2011), Vadlamudi, India, December 5, 2011, pp. 67-71.

[12] S. Swathi, S. Sushma, V. Bindusree, L Babitha, Sukesh Goud. K, S. Chinavenkateswarlu, V. Vijay, Rajeev Ratna Vallabhuni, "Implementation of An Energy-Efficient Binary Square Rooter Using Reversible Logic By Applying The Non-Restoring Algorithm," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[13] Kiran, K. Uday, Gowtham Mamidisetti, Chandra shaker Pittala, V. Vijay, and Rajeev Ratna Vallabhuni, "A PCCN-Based Centered Deep Learning Process for Segmentation of Spine and Heart: Image Deep Learning," In Handbook of Research on Technologies and Systems for E-Collaboration During Global Crises, pp. 15-26. IGI Global, 2022.

[14] Vallabhuni Vijay, V.R. Seshagiri Rao, Kancharapu Chaitanya, S. China Venkateshwarlu, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "High-Performance IIR Filter Implementation Using FPGA," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[15] Jujavarapu Sravana, S.K. Hima Bindhu, K. Sharvani, P. Sai Preethi, Saptarshi Sanyal, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Implementation of Spurious Power Suppression based Radix-4 Booth Multiplier using Parallel Prefix Adders," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-6.

[16] Ratna, Vallabhuni Rajeev, and Ramya Mariserla. "Design and Implementation of Low Power 32-bit Comparator." (2021).

[17] Vallabhuni Vijay, Kancharapu Chaitanya, T. Sai Jaideep, D. Radha Krishna Koushik, B. Sai Venumadhav, Rajeev Ratna Vallabhuni, "Design of Optimum Multiplexer In Quantum-Dot Cellular Automata," International Conference on Innovative Computing, Intelligent Communication and Smart Electrical systems (ICSES -2021), Chennai, India, September 24-25, 2021.

[18] Chandra Shaker Pittala, Vallabhuni Vijay, A. Usha Rani, R. Kameshwari, A. Manjula, D.Haritha, Rajeev Ratna Vallabhuni, "Design Structures Using Cell Interaction Based XOR in Quantum Dot Cellular Automata," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[19] S. China Venkateshwarlu, Mohammad khadir, V. Vijay, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "Optimized Design of Power Efficient FIR Filter Using Modified Booth Multiplier," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[20] G. Naveen, V.R Seshagiri Rao, Nirmala. N, Pavan kalyan. L, Vallabhuni Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Design of High-Performance Full Adder Using 20nm CNTFET Technology," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[21] Mohammad khadir, S. Shakthi, S. Lakshmanachari, Vallabhuni Vijay, S. China Venkateswarlu, P. Saritha, Rajeev Ratna Vallabhuni, "QCA Based Optimized Arithmetic Models," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[22] P. Ashok Babu, P. Sridhar, and Rajeev Ratna Vallabhuni, "Fake Currency Recognition System Using Edge Detection," 2022 Interdisciplinary Research in Technology and Management (IRTM), Kolkata, India, February 24-26, 2022, pp. 1-5.

[23] Koteshwaramma, K. C., Vallabhuni Vijay, V. Bindusree, Sri Indrani Kotamraju, Yasala Spandhana, B. Vasu D. Reddy, Ashala S. Charan, Chandra S. Pittala, and Rajeev R. Vallabhuni, "ASIC Implementation of An Effective Reversible R2B Fft for 5G Technology Using Reversible Logic," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 5-13.

[24] Vijay, Vallabhuni, Kancharapu Chaitanya, Chandra Shaker Pittala, S. Susri Susmitha, J. Tanusha, S. China Venkateshwarlu, and Rajeev Ratna Vallabhuni, "Physically Unclonable Functions Using Two-Level Finite State Machine," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 33-41.

[25] Vijay, Vallabhuni, M. Sreevani, E. Mani Rekha, K. Moses, Chandra S. Pittala, KA Sadulla Shaik, C. Koteshwaramma, R. Jashwanth Sai, and Rajeev R. Vallabhuni, "A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 27-32.

[26] Bandi Mary Sowbhagya Rani, Vasumathi Devi Majety, Chandra Shaker Pittala, Vallabhuni Vijay, Kanumalli Satya Sandeep, Siripuri Kiran, "Road Identification Through Efficient Edge Segmentation Based on Morphological Operations," Traitement du Signal, vol. 38, no. 5, Oct. 2021, pp. 1503-1508.

[27] M. Lavanya, Malla Jyothsna Priya, Ponukumatla Janet, Kavuluri Pavan Kalyan, and Vijay Vallabhuni, "Advanced 18nm FinFET Node Based Energy Efficient and High-Speed Data Comparator using SR Latch," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[28] J. Sravana, K.S. Indrani, Sankeerth Mahurkar, M. Pranathi, D. Rakesh Reddy, and Vijay Vallabhuni, "Optimised VLSI Design of Squaring Multiplier using Yavadunam Sutra through Deficiency Bits Reduction," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[29] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Low power based optimal design for FPGA implemented VMFU with equipped SPST technique," National Conference on Emerging Trends in Engineering Application (NCETEA-2011), India, June 18, 2011, pp. 224-227.

[30] Vallabhuni Vijay, and Avireni Srinivasulu, "A Novel Square Wave Generator Using Second Generation Differential Current Conveyor," Arabian Journal for Science and Engineering, vol. 42, iss. 12, 2017, pp. 4983–4990.

[31] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, and Nakka nikhil, "Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology," VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.

[32] Vijay, Vallabhuni, Chandra S. Pittala, A. Usha Rani, Sadulla Shaik, M. V. Saranya, B. Vinod Kumar, RES Praveen Kumar, and Rajeev R. Vallabhuni, "Implementation of Fundamental Modules Using Quantum Dot Cellular Automata," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 12-19.

[33] Gollamandala Udaykiran Bhargava, Vasujadevi Midasala, and Vallabhuni Rajeev Ratna, "FPGA implementation of hybrid recursive reversable box filter-based fast adaptive bilateral filter for image denoising," Microprocessors and Microsystems, vol. 90, 2022, 104520.

[34] Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, Vallabhuni Vijay, Usha Rani Anam, Kancharapu Chaitanya, "Numerical analysis of various plasmonic MIM/MDM slot waveguide structures," International Journal of System Assurance Engineering and Management, 2022.

[35] Chandra Shaker Pittala, Vallabhuni Vijay, B. Naresh Kumar Reddy, "1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications," Silicon, 2022. https://doi.org/10.1007/s12633-022-02016-8.

[36] M. Saritha, M. Lavanya, G. Ajitha, Mulinti Narendra Reddy, P. Annapurna, M. Sreevani, S. Swathi, S. Sushma, Vallabhuni Vijay, "A VLSI design of clock gated technique based ADC lock-in amplifier," International Journal of System Assurance Engineering and Management, 2022, pp. 1-8. https://doi.org/10.1007/s13198-022-01747-6

[37] B. M. S. Rani, Vallabhuni Rajeev Ratna, V. Prasanna Srinivasan, S. Thenmalar, and R. Kanimozhi, "Disease prediction based retinal segmentation using bi-directional ConvLSTMU-Net," Journal of Ambient Intelligence and Humanized Computing, 2021, pp. 1-10. https://doi.org/10.1007/s12652-021-03017-y

[38] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, M. Saritha, M. Lavanya, S. China Venkateswarlu and M. Sreevani, "ECG Performance Validation Using Operational Transconductance Amplifier with Bias Current," International Journal of System Assurance Engineering and Management, vol. 12, iss. 6, 2021, pp. 1173-1179.

[39] S. Swathi, S. Sushma, C. Devi Supraja, V. Bindusree, L. Babitha and Vallabhuni Vijay, "A Hierarchical Image Matting Model for Blood Vessel Segmentation in Retinal Images," International journal of system assurance engineering and management, vol. 13, iss. 3, 2022, pp. 1093-1101.