Journal of VLSI circuits and systems, ISSN: 2582-1458 Vol. 5, No. 1, 2023 (pp. 49-54)

RESEARCH ARTICLE WWW.VLSIJOURNAL.COM

Data Distinguisher Module Implementation using CMOS Techniques

M.R. Usikalu[1], E. N. C. Okafor[2], D. Alabi[3], G. N. Ezeh[4]

[1-4]Electrical and Electronic Engineering Department, University of Ibadan Ibadan, Nigeria

KEYWORDS:
CMOS,
Comparator,
Full Adder,
GDI,
Low power application.

ARTICLE HISTORY:
Received 14.07.2022
Accepted 15.08.2022
Published 24.09.2022

DOI:
https://doi.org/10.31838/jvcs/05.01.07

Abstract

Comparator plays a vital role in many IC applications, Microprocessors, computer systems etc. Hence it is desirable to design a comparator block with low power consumption and high speed performance .In this paper a novel architecture of 32-bit comparator using Complementary metal-oxide semiconductor logic is proposed and computed its delay and power metrics. Further it is compared with the full adder based 32-bit comparator. From the analysis we derive the comparison between proposed and the conventional comparator. The complete designing of architectures and their result analysis was done in cadence virtuoso tool at 180 nm technology. Simulation results show that there is reduce in power consumption of 90% when compared to the conventional full adder based comparator.

Author's e-mail: Mr.usikalu@ui.edu.ng, okafor.enc@ui.edu.ng, alabi.d@ui.edu.ng, ezeh.gn@ui.edu.ng

How to cite this article: Usikalu MR, Okafor ENC, Alabi D, Ezeh GN. Data Distinguisher Module Implementation using CMOS Techniques. Journal of Complementary Research, Vol. 5, No. 1, 2023 (pp. 49-54).

Introduction

Designing low power circuits has evolved CMOS technology. Among all CMOS designs Comparator is one of them with enormous applications. Comparator usually of two types. An Equality comparator suggests whether the processed bits are equal or not. On the other hand, a Magnitude Comparator, as the name says that it compares magnitude of two bits and decides whether they are equal, greater or less than to each other. Since, it defines magnitude relation the comparator block can also be interpreted as magnitude decision module.[1] It also helps in suggesting the bigger value for ease of subtraction. It is used in numerous applications such as in digital communications, in Integrated circuits applications, digital electronics etc., A 32-bit comparator usually compares two 32 bit length operands and tells whether they are equal or less than or equal to each other.[2] The novel architecture of 32-bit comparator that was discussed in this paper was designed using CMOS logic with GDI logic.[3] The Gate diffusion input is a new technique applied for low power consumption and optimized delay of a given CMOS logic design.[4] In this technique, the pmos substrate is connected to the VCC terminal and the nmos substrate is connected to ground terminal. As GDI technique is popularly known for reducing power consumption, propagation delay of the design, the proposed design follows this technique.[1-14]

This paper consists of 5 sections, in which the 2nd section deals with existing comparators so far. Section 3 includes proposed designs such as 2-bit, 4-bit, 10-bit and 32-bit comparator modules. Section 4 includes simulation results as well as comparative analysis of results. Section 5 includes conclusion and future scope of proposed design.

Existing Comparators

A Comparator usually performs subtraction operation in order to determine its operands relation. It can also be performed with help of carry look-ahead logic in which the relation between operands is defined by generate bits and propagate bits.[5] The existing designs include serial and parallel structured comparators.[6] The disadvantage with these comparators is that they provide less efficiency with respective to large inputs. The novel structure includes of 32-bit comparator is implemented by using lower range of comparators such as 10 and 4, 2 bit comparators respectively. The lower range 10-bit and 4-bit comparators are designed with help of cascading 4-bit and 2-bit comparators.[15-25]

The 32-bit comparator is designed and implemented using Cadence virtuoso tool at 180 nm technology and is compared with the Raman's Full adder based 32-bit comparator architecture.[7] The Proposed architecture of Full adder based 32-bit comparator is as shown in the Fig. 1.

The Fig. 1 design works on the principle of adder. The results obtained with two inputs A, B are basis for generations of all the outputs. When A, B inputs generates, carry out generated is '1' and sum as non-zero then it is considered as A>B condition. Similarly for equal than condition, carry out should be logic 1 and sum is equal to 0. For less than condition, carry out should be equal to 0.[26-32]

The average power, delay and the power-delay product has been calculated. Usually these factors are mostly calculated as they define the optimal circuit performance. The major parameters in digital design are power, speed. If a design meets the requirements of speed it will not satisfy the requirement of power consumption and vice versa. The main aim of this the proposed design is to bring down the power metric down for usage of low power applications. Hence, in this paper a 32-bit comparator is designed using the 2,4,10 bit comparators focusing on less power consumption. Later on the calculated values of metrics are tabulated.[33-36]

Proposed Model

The Proposed model which is a 32-bit comparator is designed from its lower order designs such as 2-bit, 4-bit, 10-bit modes respectively.[8] Therefore, these designs play an important role in power consumed by the 32-bit comparator.

2-bit comparator

A 2-bit comparator as name suggests compares magnitude of two bit length variables [9]. It is realized using combinations of AND, OR gate combinations respectively as shown in the following Fig 2. The conventional 2-bit comparator equations are as follows [10].

1. A= B (equal condition): A1, B1 A0, B0
   Boolean expression: x1x0: $xi = A_iB_i + A_i'B_i'$
2. A greater than B
   Boolean expression: $A_1B_1' + x_1A_0B_0'$
3. A less than B
   Boolean expression: $A_1'B_1 + x_1A_0'B_0$

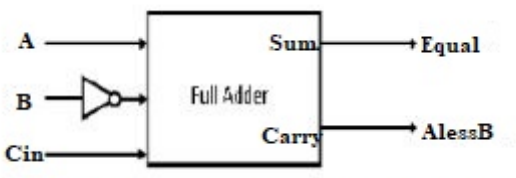


Fig. 1: (a) First picture; (b) Second picture

4-bit comparator

The Comparator that is required to compare a length of 4-bit of each variable is a 4-bit comparator [11]. The 4-bit comparator is implemented irrespective of Boolean expressions. It is designed using three 2-bit comparators successively. For the succession comparators the less than and greater than outputs are rippled for generating the required logic as shown in Fig. 2.[37]-[38]

10-bit comparator

The 10-bit comparator perform operation totally on 20 bits i.e. it compares two 10 bit length variables. It is usually generated using boolean expressions as that of 2-bit comparator. In this case, the design implementation is done using three 4-bit comparators[11] as shown in Fig. 3.

32-bit comparator

The 32-bit comparator usually compares two 32 bit length variables. The design methodology proposed in this design is similar to N-bit parallel adder. A Parallel adder is designed using single bit full adder modules. In the same way, the proposed 32-bit comparator which is completely a novel architecture was implanted using low bit comparators such as 10, 4, 2 bit comparators which was seen in Fig. 3 and Fig. 4.

The only difference between a conventional comparator and the proposed one is that the conventional one designed through logic equations whereas the proposed one follows rippling of bits. In this design, the output bits of A>B (A greater than B), A<B (A less than B) that are generated at one comparator module is rippled to another[12]. In this design, the least significant bits are compared first and later the most significant bits are compared. So, the final

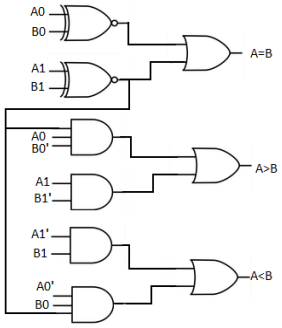


Fig. 2: Design of 2-bit Comparator

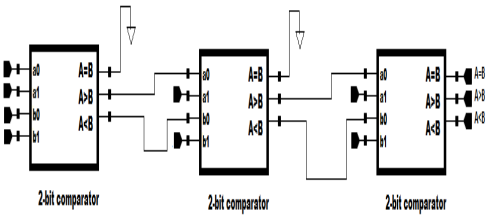


Fig. 3: Design of 4-bit Comparator

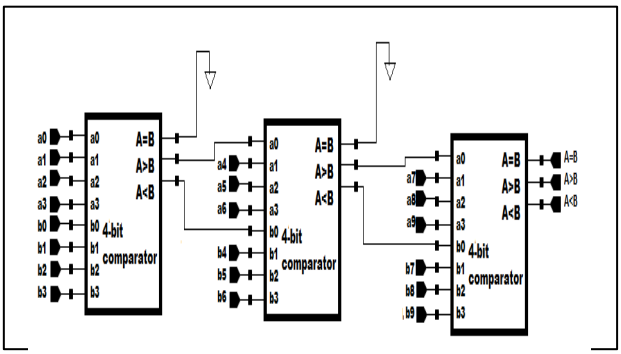


Fig. 4L Design of 10-bit Comparator

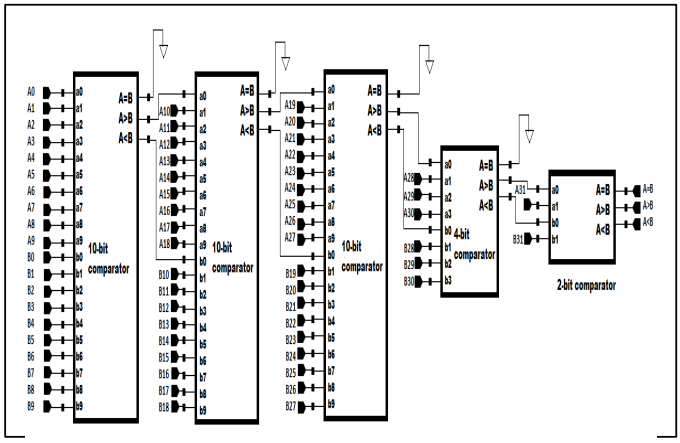


Fig. 5: Design of 32-bit Comparator

comparison of bits depends on initial stages of compared bits.[13]

The figure 5 depicts the proposed 32-bit comparator

Results and Simulations

In this section, the Power and delay metrics [14] can be seen and compared with Raman's design of Full adder based 32-bit comparator using full adder which was implemented in Xilinx software.

Simulation Results

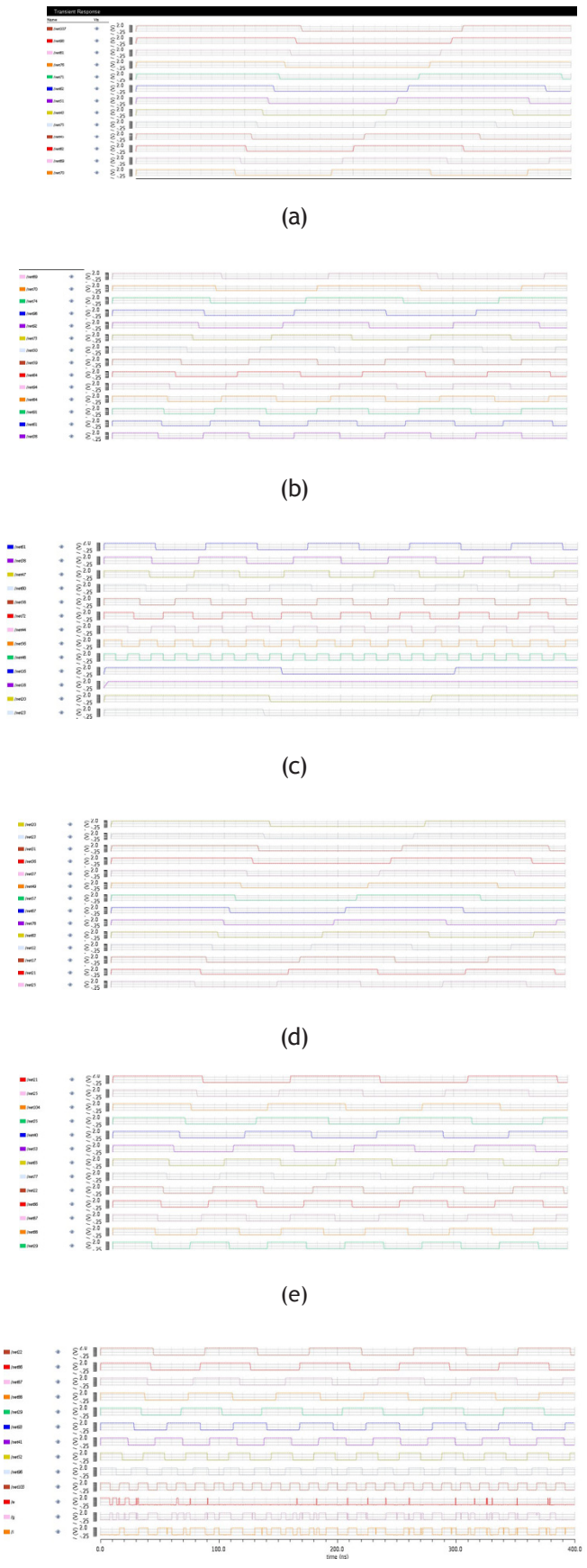
The functionality of the proposed design is tested by providing pulse signal with logic 1 as 1.8 volts and logic 0 as 0 volts respectively. The Variation of inputs is provided by giving different period and Pulse width to the signals.

The waveforms of 32-bit comparator are shown Fig. 6.

The figures up to 6-e defines inputs from (A0-A31) and (B0-B31), respectively. The final results of A>B, A<B, A=B is simulated in Fig.6 (e).

Comparative analysis of results

The overall delay of 32-bit comparator is tabulated using Cadence virtuoso tool. The delay calculations specify the amount of time required for the output generation after the inputs has been applied. The delay between each and



(a)

(b)

(c)

(d)

(e)

(f)

Fig. 6: Waveforms of 32-bit Comparator

Table 1: Delay Of 32-Bit Comparator

	OUTPUTS		
INPUTS	*A<B*	*A=B*	*A>B*
A0	15.76E-9	7.42 E-9	7.341 E-9
A1	15.77 E-9	7.434 E-9	7.355 E-9
A2	15.78 E-9	7.448 E-9	7.369 E-9
A3	15.8 E-9	7.462 E-9	7.383 E-9
A4	15.81 E-9	7.476 E-9	7.397 E-9
A5	15.82 E-9	7.49 E-9	7.411 E-9
A6	1584 E-9	7.503 E-9	7.425 E-9
A7	15.83 E-9	7.517 E-9	7.439 E-9
A8	15.87 E-9	7.531 E-9	7.452 E-9
A9	15.88 E-9	7.545 E-9	7.466 E-9
A10	15.89 E-9	7.55 E-9	7.48 E-9
A11	15.91 E-9	7.573 E-9	7.494 E-9
A12	15.92 E-9	7.587 E-9	7.508 E-9
A13	15.94 E-9	7.601 E-9	7.522 E-9
A14	15.95 E-9	7.615 E-9	7.536 E-9
A15	15.96 E-9	7.628 E-9	7.55 E-9
A16	15.98 E-9	7.642 E-9	7.564 E-9
A17	15.99 E-9	7.656 E-9	7.577 E-9
A18	16.01 E-9	7.67 E-9	7.591 E-9
A19	16.02 E-9	7.684 E-9	7.605 E-9
A20	16.03 E-9	7.698 E-9	7.619 E-9
A21	16.04 E-9	7.703 E-9	7.625 E-9
A22	16.05 E-9	7.712 E-9	7.633 E-9
A23	16.05 E-9	7.717 E-9	7.639 E-9
A24	16.06 E-9	7.726 E-9	7.647 E-9
A25	16.07 E-9	7.731 E-9	7.652 E-9
A26	16.07 E-9	7.74 E-9	7.661 E-9
A27	16.09 E-9	7.753 E-9	7.675 E-9
A28	16.10 E-9	7.767 E-9	7.689 E-9
A29	16.12 E-9	7.781 E-9	7.702 E-9
A30	16.13 E-9	7.79 E-9	7.716 E-9
A31	16.14 E-9	7.809 E-9	7.73 E-9
B0	15.76 E-9	7.426 E-9	7.347 E-9
B1	14.78 E-9	6.448 E-9	6.369 E-9
B2	15.79 E-9	7.453 E-9	7.375 E-9
B3	15.80 E-9	7.467 E-9	7.389 E-9
B4	15.82 E-9	7.481 E-9	7.402 E-9
B5	15.83 E-9	7.495 E-9	7.416 E-9
B6	15.84 E-9	7.509 E-9	7.43 E-9
B7	15.86 E-9	7.523 E-9	7.444 E-9
B8	15.87 E-9	7.537 E-9	7.458 E-9
B9	15.89 E-9	7.551 E-9	7.472 E-9
B10	15.90 E-9	7.565 E-9	7.486 E-9
B11	15.91 E-9	7.578 E-9	7.50 E-9
B12	15.93 E-9	7.592 E-9	7.514 E-9
B13	15.94 E-9	7.606 E-9	7.527 E-9
B14	15.96 E-9	7.62 E-9	7.541 E-9
B15	15.97 E-9	7.634 E-9	7.555 E-9
B16	15.98 E-9	7.648 E-9	7.569 E-9
B17	16.0 E-9	7.662 E-9	7.583 E-9
B18	16.01 E-9	7.676 E-9	7.597 E-9
B19	16.02 E-9	7.69 E-9	7.611 E-9
B20	16.04 E-9	7.701 E-9	7.622 E-9
B21	16.04 E-9	7.706 E-9	7.627 E-9
B22	16.05 E-9	7.715 E-9	7.636 E-9
B23	16.06 E-9	7.72 E-9	7.641 E-9
B24	16.06 E-9	7.728 E-9	7.65 E-9
B25	16.07 E-9	7.734 E-9	7.655 E-9
B26	16.08 E-9	7.742 E-9	7.664 E-9
B27	16.09 E-9	7.759 E-9	7.68 E-9
B28	16.11 E-9	7.773 E-9	7.694 E-9
B29	16.12 E-9	7.787 E-9	7.708 E-9
B30	16.14 E-9	7.801 E-9	7.722 E-9
B31	16.15 E-9	7.815 E-9	7.736 E-9
Average Delay			10.34ns

Table 2: Comparison Between Proposed And Full Adder Based 32-Bit Comparator

Design	*Power (mW)*	*Delay (nS)*	*Power-delay product (PJ)*
Full adder based Comparator	151	5.23	789.73
Proposed Comparator	15.4	10.34	157.168

every input to generate the required output has been noted.

Power is an essential metric that is calculated for defining the performance of any logic circuitry [11]. The power consumption of the proposed 32-bit comparator is 90% lesser than the Raman's Full adder based comparator architecture which is tabulated in table 2.

The Power-delay product specifies the amount of energy consumption per performed or switching event. It is usually calculated by multiplying the power consumed with the average delay of the switching event.

The comparisons between proposed and full adder based 32-bit comparator has been laid as shown in table2.

The Comparison table shows that there is reduce in power consumption nearly 90%, Delay has 50% increased. This shows the fact that for a circuit to be designed perfectly, it has to either bear disadvantages regarding power or delay. The power-delay product that ensures the efficiency and overall performance of proposed design is reduced nearly 80% with respective to the full based design.

Conclusion

In this paper, a novel architecture of 32-bit is proposed. The design of this architecture is implemented in Cadence virtuoso tool at 180 nm technology. The simulated results such as power, delay and power-delay product were produced with 1.8 volts supply. The Gate Diffusion Input technique enhances the simulation results by reducing power consumption [15]. The results depicts that the proposed design provides 90% less power consumption and some compatible delay. As in technology low power consumption became a vital factor, the proposed design enables that fact.

References

[1] S. Swathi, S. Sushma, V. Bindusree, L Babitha, Sukesh Goud. K, S. Chinavenkateswarlu, V. Vijay, Rajeev Ratna Vallabhuni, "Implementation of An Energy-Efficient Binary Square Rooter Using Reversible Logic By Applying The Non-Restoring Algorithm," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[2] Kiran, K. Uday, Gowtham Mamidisetti, Chandra shaker Pittala, V. Vijay, and Rajeev Ratna Vallabhuni, "A PCCN-Based Centered Deep Learning Process for Segmentation of Spine and Heart: Image Deep Learning," In Handbook of Research on Technologies and Systems for E-Collaboration During Global Crises, pp. 15-26. IGI Global, 2022.

[3] Vallabhuni Vijay, V.R. Seshagiri Rao, Kancharapu Chaitanya, S. China Venkateshwarlu, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "High-Performance IIR Filter Implementation Using FPGA," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[4] Jujavarapu Sravana, S.K. Hima Bindhu, K. Sharvani, P. Sai Preethi, Saptarshi Sanyal, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Implementation of Spurious Power Suppression based Radix-4 Booth Multiplier using Parallel Prefix Adders," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-6.

[5] Chandra Shaker Pittala, Vallabhuni Vijay, A. Usha Rani, R. Kameshwari, A. Manjula, D.Haritha, Rajeev Ratna Vallabhuni, "Design Structures Using Cell Interaction Based XOR in Quantum Dot Cellular Automata," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[6] S. China Venkateshwarlu, Mohammad khadir, V. Vijay, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "Optimized Design of Power Efficient FIR Filter Using Modified Booth Multiplier," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[7] G. Naveen, V.R Seshagiri Rao, Nirmala. N, Pavan kalyan. L, Vallabhuni Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Design of High-Performance Full Adder Using 20nm CNTFET Technology," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[8] Mohammad khadir, S. Shakthi, S. Lakshmanachari, Vallabhuni Vijay, S. China Venkateswarlu, P. Saritha, Rajeev Ratna Vallabhuni, "QCA Based Optimized Arithmetic Models," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[9] P. Ashok Babu, P. Sridhar, and Rajeev Ratna Vallabhuni, "Fake Currency Recognition System Using Edge Detection," 2022 Interdisciplinary Research in Technology and Management (IRTM), Kolkata, India, February 24-26, 2022, pp. 1-5.

[10] Koteshwaramma, K. C., Vallabhuni Vijay, V. Bindusree, Sri Indrani Kotamraju, Yasala Spandhana, B. Vasu D. Reddy, Ashala S. Charan, Chandra S. Pittala, and Rajeev R. Vallabhuni, "ASIC Implementation of An Effective Reversible R2B Fft for 5G Technology Using Reversible Logic," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 5-13.

[11] Vijay, Vallabhuni, Kancharapu Chaitanya, Chandra Shaker Pittala, S. Susri Susmitha, J. Tanusha, S. China Venkateshwarlu, and Rajeev Ratna Vallabhuni, "Physically Unclonable Functions Using Two-Level Finite State Machine," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 33-41.

[12] Vijay, Vallabhuni, M. Sreevani, E. Mani Rekha, K. Moses, Chandra S. Pittala, KA Sadulla Shaik, C. Koteshwaramma, R. Jashwanth Sai, and Rajeev R. Vallabhuni, "A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 27-32.

[13] Vijay, Vallabhuni, Chandra S. Pittala, A. Usha Rani, Sadulla Shaik, M. V. Saranya, B. Vinod Kumar, RES Praveen Kumar, and Rajeev R. Vallabhuni, "Implementation of Fundamental Modules Using Quantum Dot Cellular Automata," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 12-19.

[14] Gollamandala Udaykiran Bhargava, Vasujadevi Midasala, and Vallabhuni Rajeev Ratna, "FPGA implementation of hybrid recursive reversable box filter-based fast adaptive bilateral filter for image denoising," Microprocessors and Microsystems, vol. 90, 2022, 104520.

[15] Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, Vallabhuni Vijay, Usha Rani Anam, Kancharapu Chaitanya, "Numerical analysis of various plasmonic MIM/MDM slot waveguide structures," International Journal of System Assurance Engineering and Management, 2022.

[16] Ratna, Vallabhuni Rajeev, and Ramya Mariserla. "Design and Implementation of Low Power 32-bit Comparator." (2021).

[17] Vallabhuni Vijay, Kancharapu Chaitanya, T. Sai Jaideep, D. Radha Krishna Koushik, B. Sai Venumadhav, Rajeev Ratna Vallabhuni, "Design of Optimum Multiplexer In Quantum-Dot Cellular Automata," International Conference on Innovative Computing, Intelligent Communication and Smart Electrical systems (ICSES -2021), Chennai, India, September 24-25, 2021.

[18] S. Sushma, S. Swathi, V. Bindusree, Sri Indrani Kotamraju, A. Ashish Kumar, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "QCA Based Universal Shift Register using 2 to 1 Mux and D flip-flop," IEEE 2021 International Conference on Advances

in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[19] M. Sreevani, S. Lakshmanachari, B. Manvitha, Y.J.N. Pravalika, T.Praveen,V.Vijay, Rajeev Ratna Vallabhuni, "Design of Carry Select Adder Using Logic Optimization Technique," IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[20] M. Saritha, Chelle Radhika, M. Narendra Reddy, M. lavanya, A. Karthik, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Pipelined Distributive Arithmetic-based FIR Filter Using Carry Save and Ripple Carry Adder," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[21] Chandra Shaker Pittala, Vallabhuni Vijay, B. Naresh Kumar Reddy, "1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications," Silicon, 2022. https://doi.org/10.1007/s12633-022-02016-8.

[22] M. Saritha, M. Lavanya, G. Ajitha, Mulinti Narendra Reddy, P. Annapurna, M. Sreevani, S. Swathi, S. Sushma, Vallabhuni Vijay, "A VLSI design of clock gated technique based ADC lock-in amplifier," International Journal of System Assurance Engineering and Management, 2022, pp. 1-8. https://doi.org/10.1007/s13198-022-01747-6

[23] B. M. S. Rani, Vallabhuni Rajeev Ratna, V. Prasanna Srinivasan, S. Thenmalar, and R. Kanimozhi, "Disease prediction based retinal segmentation using bi-directional ConvLSTMU-Net," Journal of Ambient Intelligence and Humanized Computing, 2021, pp. 1-10. https://doi.org/10.1007/s12652-021-03017-y

[24] J. Sravana, K.S. Indrani, Sankeerth Mahurkar, M. Pranathi, D. Rakesh Reddy, and Vijay Vallabhuni, "Optimised VLSI Design of Squaring Multiplier using Yavadunam Sutra through Deficiency Bits Reduction," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[25] L. Babitha, U. Somanaidu, CH. Poojitha, K. Niharika, V. Mahesh, and Vallabhuni Vijay, "An Efficient Implementation of Programmable IIR Filter for FPGA," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[26] K. C. Koteswaramma, Ande Shreya, N. Harsha Vardhan, Kantem Tarun, S. China Venkateswarlu, and Vallabhuni Vijay, "ASIC Implementation of division circuit using reversible logic gates applicable in ALUs," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[27] Vallabhuni Vijay, J. Sravana, K.S. Indrani, G. Ajitha, A. Prashanth, K. Nagaraja, K.C. Koteswaramma, C. Radhika, M. Hima Bindu, N. Manjula, "A SYSTEM FOR CONTROLLING POSITIONING ACCORDING TO MOVEMENT OF TERMINAL IN WIRELESS COMMUNICATION BASED ON AI INTERFACE," The Patent Office Journal No. 50/2021, India. Application No. 202141055995 A.

[28] Dr. L.V. Narasimha Prasad, Dr. Vijay Vallabhuni, Dr. S. China Venkateswarlu, Dr. V. Vhandra Jagan Mohan, Ms. P. Sruthilaya, Mr. K. Tarun Kumar, Mr. B. Raju, Mr. P. Ravinder, "Garbage Collector with Smart Segregation and Method of Segregation Thereof," The Patent Office Journal No. 04/2022, India. Application No. 202141062270 A.

[29] Sravana, J., K. S. Indrani, M. Saranya, P. Sai Kiran, C. Reshma, and Vallabhuni Vijay, "Realısatıon of Performance Optımısed 32-Bıt Vedıc Multıplıer," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 14-21.

[30] V. Vijay, J. Prathiba, S. Niranjan Reddy, V. Raghavendra Rao, "Energy efficient CMOS Full-Adder Designed with TSMC 0.18µm Technology," International Conference on Technology and Management (ICTM-2011), Hyderabad, India, June 8-10, 2011, pp. 356-361.

[31] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Optimal design of VLSI implemented Viterbi decoding," National conference on Recent Advances in Communications & Energy Systems, (RACES-2011), Vadlamudi, India, December 5, 2011, pp. 67-71.

[32] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Low power based optimal design for FPGA implemented VMFU with equipped SPST technique," National Conference on Emerging Trends in Engineering Application (NCETEA-2011), India, June 18, 2011, pp. 224-227.

[33] Vallabhuni Vijay, and Avireni Srinivasulu, "A Novel Square Wave Generator Using Second Generation Differential Current Conveyor," Arabian Journal for Science and Engineering, vol. 42, iss. 12, 2017, pp. 4983–4990.

[34] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, and Nakka nikhil, "Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology," VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.

[35] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, M. Saritha, M. Lavanya, S. China Venkateswarlu and M. Sreevani, "ECG Performance Validation Using Operational Transconductance Amplifier with Bias Current," International Journal of System Assurance Engineering and Management, vol. 12, iss. 6, 2021, pp. 1173-1179.

[36] S. Swathi, S. Sushma, C. Devi Supraja, V. Bindusree, L. Babitha and Vallabhuni Vijay, "A Hierarchical Image Matting Model for Blood Vessel Segmentation in Retinal Images," International journal of system assurance engineering and management, vol. 13, iss. 3, 2022, pp. 1093-1101.

[37] Bandi Mary Sowbhagya Rani, Vasumathi Devi Majety, Chandra Shaker Pittala, Vallabhuni Vijay, Kanumalli Satya Sandeep, Siripuri Kiran, "Road Identification Through Efficient Edge Segmentation Based on Morphological Operations," Traitement du Signal, vol. 38, no. 5, Oct. 2021, pp. 1503-1508.

[38] M. Lavanya, Malla Jyothsna Priya, Ponukumatla Janet, Kavuluri Pavan Kalyan, and Vijay Vallabhuni, "Advanced 18nm FinFET Node Based Energy Efficient and High-Speed Data Comparator using SR Latch," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.