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Fundamental Design Approach: Realization of Decoder Block for Secured Transmission

Fahad Al-Jame[1], Rana A. Al-Fares[2], Wesam Ali[3], H. Ashour[4], Nimer Murshid[5]

[1-5]School of Electrical Engineering, Kuwait Institute for Scientific Research (KISR), P.O. Box 24885 Safat, Kuwait

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Abstract

VLSI technology is essential for chip fabrication, and 3 to 8 decoder circuits are used in electronic gadgets; consistency of design, small, fast, in this proposed circuit, 3 to 8 decoder is implemented using 20nm CNTFET technology. 3 to 8 decoders are the key segments in some real-time applications. For the most recent couple of years, the minuscule size of MOSFET, which is under many nanometers, made some operational issues, for example, expanded entryway oxide leakage, intensified intersection leakage, high sub-limit conduction. The proposed model is recreated utilizing Cadence virtuoso with 20nm CNTFET nodes.

Author's e-mail: Fah.al-ja@kisr.edu.kw, ranaa.al@kisr.edu.kw, wesamal.i@kisr.edu.kw, ashour.h@kisr.edu.kw, nimer.mur@kisr.edu.kw

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Introduction

The increase in demand for ultra-high-speed processors, lower power consumptions of integrated circuits and smaller dimensions has evolved the technology scaling and challenging issues for the designers. CNFET built on single-walled semiconducting has led to complement silicon and extended CMOS technology scaling at sub-10nm technology nodes. Semiconducting carbon nanotubes based on their properties like excellent carrier mobility, mean free path and improved electrostatics for nanoscales as because of this, CNTs are the best replacement for silicon.[1-11]

Types of CNFETs

The two main types of CNFETs are back-gated CNFET and Top-gated CNFET.

Back-gated CNFETs

Tans introduced the CNFETs to demonstrate specialized switching ways and made the CNFETs in research progressions. Earlier, CNFETs are back-ended that involve strips parallelly on metal over a silicon diode substrate in random pattern depositing CNTs on top. The CNTs of two metal strips are formed consists of the preconditions of field effect transistor. The metal strip one is 'source', and the second is 'drain' makes contact ends. A metal contact is made on the back which is used as gate oxide is of silicon oxide substrate.[12-19]

This technique has some drawbacks as for further improvement introduced a top-gated structure CNFETs. The first is a metal contact, the nanotube on the top was minimal contact to the CNT, and the contact area is very small. A Schottky barrier forms at the metal-semiconductor interface is due to the semiconducting nature of the CNT increase the contact resistance. The second is due to back gate device geometry as the switching of the device on and off was made difficult at low voltage due to thickness, and the fabrication process led to poor contact between the gate dielectric and CNT.[20-27]

Top-gated CNFETs

To increase the device performance, CNFET has designed with a top-gated structure. The structure is made by using a carbon nanotube on the oxidized wafer. Each nanotube is located via atomic force microscopy. High-resolution beam lithography is used to isolate the source and drain contacts. At the top of the nanotube, a thin top-gate dielectric is deposited using atomic layer deposition or evaporation. Eventually, the top gate contact on gate dielectric.[28-37]

On a wafer, an array of the top-gated CNTFET can be fabricated, and unlike in the back gated case, the gate contacts are electrically isolated from each other. Also,

a larger electric field can be generated with respect to the nanotube using a lower gate voltage due to the gate electric's thinness. Thus, the advantages mean top-gated device are generally preferred over back-gated CNTFET despite their more complex fabrication process.[38-47]

CNTFET Characteristics and Modeling

CNTFETs with device characteristics have been illustrated. In these transistors, the drain and source metal contacts are directly attached to the intrinsic nanotube channel, as these type of transistors can be known as Schottky barrier CNTFETs.[7] The SBCNTFETs show high gate voltage for electron conduction and low gate voltage for hole conduction when the metal Fermi level is pinned at the centre of the gap.[8]

The essential operation of carbon nanotube transistor is like the metal oxide semiconductor FET as the electrons move from the source terminal to the drain terminal and the gate terminal is used as the controlling region for the flow of current in the channel, and the transistor is in the state of OFF if the gate voltage is zero.[9] In the modelling issues, the preponderance of CNFETs models available is numerical as they cannot be implemented in modelling language to implement in electronic circuits such as Verilog-A, VHDL-AMS or SPICE. In general, the modelling of the device implies a solution for a set of partial differential equations. The operation of different structure is considered that as Schottky barrier CNTFET and the Metal Oxide Semiconductor Field Effect Transistor -Like CNTFET.[10]

Schottky-barrier CNTFET

In the Schottky-barrier CNTFET channel region used is intrinsic CNT that is affix to source and drain metal, at the junction forms Schottky barriers. The carbon nanotube transistor operates an unusual Schottky barrier transistor such that transistor operation depends on changing contact resistance instead of the channel conductance.[5] In a Partially gated Carbon nanotube transistor, the nanotube is uniformly doped with ohmic contacts at the ends and it of two types that is n-type and p-type depending on doping, whereas the doped source-drain CNTFET is three areas, one is p-type, second is n-type, and the third is the built-in gate. ON current is limited by charges caused in the gate's channel and not by the source doping. It either operates in enhancement mode or depletion mode of pure p-type or N-type with a principle of when the gate potential is applied, the height modulation of barrier is done.[11]

Metal Oxide Semiconductor Field Effect Transistor-Like CNTFET

This device's structure is a bit different from SB-CNTFET, where it has been highly doped regions are used. In this, the drain current is controlled by the gate terminal by changing several charges induced through the channel. It has many pros over SB-CNTFET as it can eliminate ambipolar conduction and furnish lengthy channel length such as the density of metal caused gap is significantly/ famously reduced. The (related to things that slowly feed off of and weaken other things) capacitance across the source and gate terminal is highly reduced and because of this increases the speed of operation of the transistor.

The MOSFET, like CNTFET operates like Schottky-barrier-CNTFET during ON condition with negative Schottky barrier height, and hence it transfers high ON current than SB-CNTFET. Faster operation is accomplished because the length across the drain/ source and gate terminals can be parted by the length of the source to drain, which reduces the parasitic capacitance and, because of this, increases the speed.[12-13]

Proposed Circuit: Design and Realization

In the design process, the combinational circuit is considered that is the binary decoder which is a combinational logic circuit that converts n coded binary inputs to the 2n outputs. The combinational circuits have many applications like data multiplexing, demultiplexing, seven-segment display, encoder and memory address decoding.

In the VLSI system, power consumption is an important consideration. Here is the standard 3:8 decoder constructed using NAND gate, and for the complimentary operation, the Inverter test bench is used, as shown in Fig. 1. There are different colours used for indicating the terminals. The green colour line indicates the ground terminal, V_{DD} terminal is indicated by the red colour line. The A, B, C are the inputs, and the DO to D7 are output terminals indicated by pink and blue colours, respectively.

The 3:8 decoder is constructed using a NAND gate, and for the complementary operation, an inverter test bench

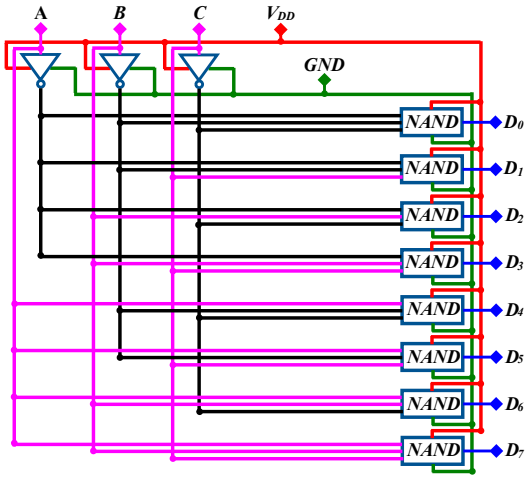

Fig. 1: Conventional decoder block diagram using NAND gates

is used. The operation of the decoder is when the input is ABC=100, and the D3 line becomes zero NAND all other lines become one. The leakage current is reduced by connecting a sleep transistor with NAND gate, as shown in Fig. 2.

The cluster technique is used in the conventional circuits because sleep transistors are not used; instead of that, a standard gate is used, which is connected among all NAND gates to the ground terminal, as shown in Fig. 3. This technique is used to reduce the area and work the decoder the same as a standard decoder.

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The circuit of Fig. 4 is similar to the cluster circuit. The one difference is body biasing circuit is used instead of a sleep transistor. The Threshold voltage of the transistor is modified by the body terminal of the biasing circuit.

In the circuit of Fig. 5, a source bias circuit is used instead of a sleep transistor. The standard input is connected to the voltage supply, the output of the inverter is connected to the source terminal, and the body terminal

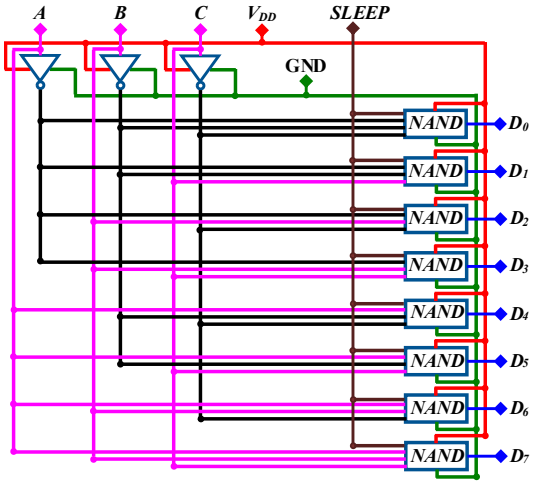

Fig. 2: Conventional decoder block diagram using NAND gates with sleep transistor

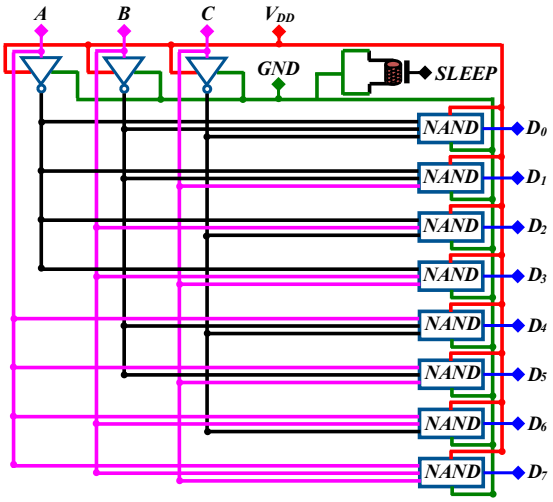

Fig. 3: Conventional decoder block diagram using NAND gates with cluster circuit

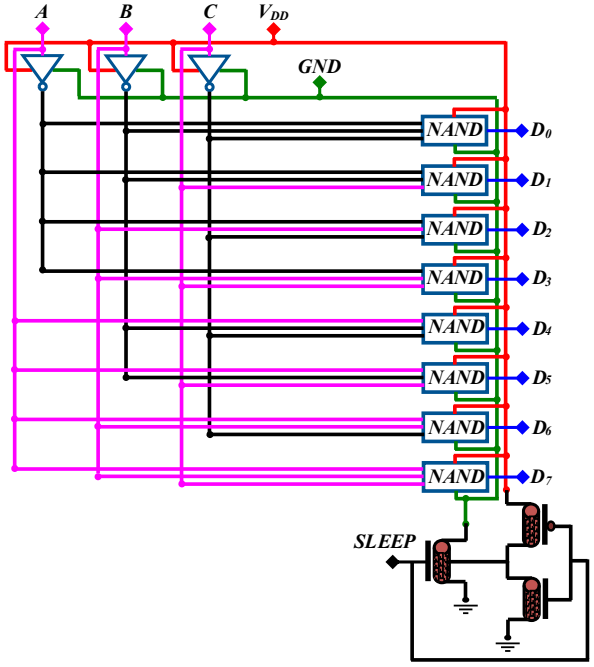

Fig. 4: Decoder block diagram using NAND gates with body bias circuit

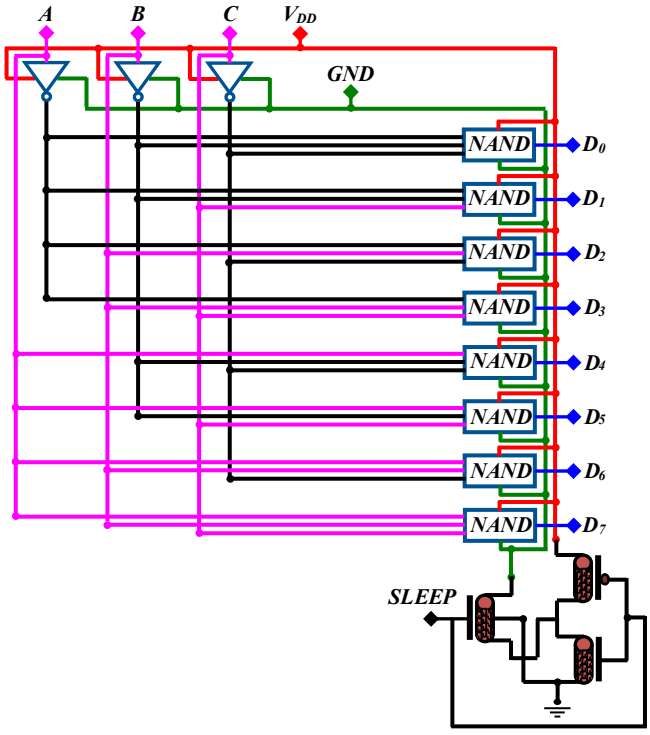

Fig. 5: Decoder block diagram using NAND gates with source biasing circuit

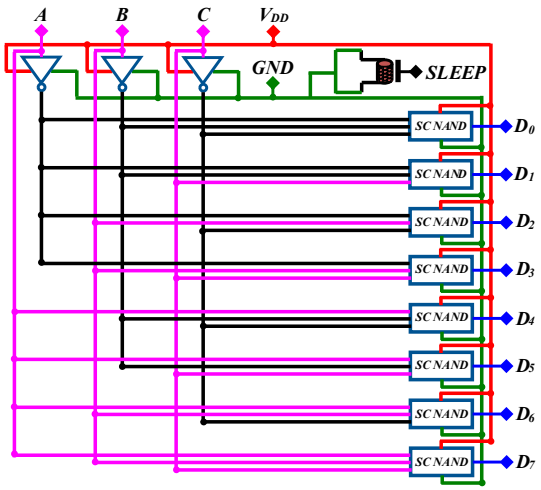

Fig. 6: Decoder block diagram using NAND gates with source coupled circuit.

is grounded. Sleep transistor threshold voltage is used to control the source terminal, which controls the output of the inverter circuit.

In this source coupled method, the third terminal of the NAND gate is connected to the inverter circuit input as shown in Fig. 6, source terminal of NMOS is connected to the inverter circuit.

Design of Efficient Decoder circuit consists of following novel techniques:

- The Decoder circuit designed without utilizing a sleep transistor using NAND gate
- The Decoder circuit designed utilizing a sleep transistor using NAND gate
- The Decoder circuit designed utilizing Cluster circuit using NAND gate
- The Decoder circuit designed utilizing a body biasing circuit using NAND gate
- The Decoder circuit designed utilizing a gate-source biasing circuit using NAND gate

The proposed designs are modeled and developed in a cadence virtuoso environment, and all the models have exhibited more significant improvement in terms of speed, power dissipation, power delay product (PDP) and energy-delay product (EDP). A sample transient response of the proposed circuit is depicted in Fig. 7.

The cadence virtuoso results for the 20nm CNTFET models at ultra-low supply voltages for the proposed results are given in the Table 1. For the supply voltages from 0.1V to 1V has applied for the above adopted novel circuits and their resultant PDP and EDP values shown a greater improvements in contrast to the standard decoder circuits developed using other conventional transistors.

Six novel approaches are considered for power minimization in the essential data encryption blocks of decoder modules. All these six methodologies are

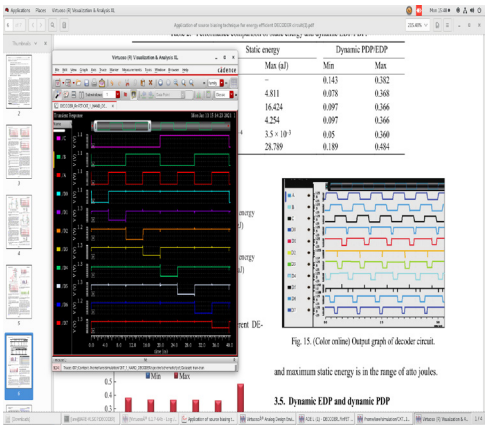

Fig. 7: Transient response of circuit shown in Fig. 1

Observations of the Proposed Designs

Proposed Design	Delay (ps)	Power (nW)	PDP (x10-18J)	EDP (x10-30Js)
Fig. 1	110	3.62	0.392	43.56
Fig. 2	82	3.74	0.298	25.15
Fig. 3	91	3.91	0.356	32.38
Fig. 4	93	4.87	4.464	42.11
Fig. 5	60	4.76	2.820	17.14
Fig. 6	128	4.49	5.850	73.55

implemented using 20nm CNTFET nodes in Cadence virtuoso. The circuits are simulated to validate the vital performance metrics of power dissipation and delay in addition to the other important specifications of leakage current and static power dissipation.

The body biasing technique of Fig. 3 has exhibited a progress of 4% and 29% for dynamic power consumption and delay, respectively. Similar kind of development has observed for the clustering method of circuit shown in Fig. 4. The source biasing used in Fig. 5 has raised a speed improvement at 57% and the same kind of speed advantage has observed from source coupled mechanism given in Fig. 6.

Conclusion

In this proposed method, the decoder circuit presented with two techniques that are cluster technique and source coupled technique. The CNTFET has better control over the channel, have better values of threshold, high electron ability to move around, current density, linearity and transconductance. In different decoder design techniques, the cluster technique and source coupled technique are the better techniques for memory array application, where the source biasing decoder circuit configuration fulfils all the requirements. The circuit speed has been increased, which is an added fifty-seven percentage improvement as compared to other techniques. This has a minor delay,

which is suitable for decoder designing in row and column. The proposed body biasing technique and clustering technique has four percentage improvements in dynamic power and dynamic energy, twenty-nine percentage improvement in delay calculation. There is an improvement of eleven percentage in static energy in the body biasing technique and leakage current.

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