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Fundamental Digital Module Realization Using RTL Design for Quantum Mechanics

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Abstract

Calculation of square root will be an essential mathematical operation that will have broad applications. In Hardware, the square root will be designed in order to gain power which will be quite low. Similarly, there are also other advantages that comes with gaining of low power that is high speed and also low area. A trade-off will also occur with the three metrics which is quite natural. As we know that the present technology is very advanced so it will aim for low power and architectural modification will be required by the relative designs. This sheet represents an energy efficient square rooter by using reversible logic. (RCSM) Reversible Controlled Subtract Multiplexer will be designing and it also plays an important part in implementing the binary square rooter. Saimur Rahman Gate will also be implementing the binary square rooter in order to improve and develop it. The Improvements such as cost of the quanta, inputs given by constants and also garbage outputs. The approaches such as conventional approach and SRG are used for designing the binary square rooter and it will be completed using non-restoring algorithm. Xilinx Software will be responsible for carrying out simulations and Synopsys Design Compiler will be the factor for obtaining power. The gate count which has been 75 will be decreased to 35. There will be an improvement of 20% in terms of power which will be obtained in this paper.

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Introduction

Square root is considered to be one of the essential mathematical operation. They are involved in a wide range of applications namely data processing, computer graphics, DSP(digital signal processing) a global positioning system (GPS), and many mathematical calculations. For portable and wireless devices, Low power is the basic necessity. Square rooters in use for many years for various purposes. We use reversible logic in our design to attain low power. The number of input ports and output port is not uniform in Irreversible logics, and therefore it resulted in the loss of information bits. A single bit present in the information dissipates kTln2 Joules of energy which was proposed by Launders Theorem.[1] To avoid the loss of information bits and energy loss, reversible logic is used.[2] The loss of heat can be avoided by keeping the number of input and output ports present in the reversible logic in a uniform manner. Power consumption will be reduced in square rooter. A reversible nonlinear feedback shift register will be developed by a low power Authors in.[3]

The calculation of square root can be performed either by restoring or non-restoring using the digit-by-digit technique. The methods proposed by Newton Rapshon and Goldschmidt[4] requires more hardware resources and has many steps involved than the digits by digits method. More hardware resources are necessary for restoring the approach. Hardware will be consumed less in the non-restoring process,[5] when compared to restoring practice. So thereby, Square root will select non-restoring process. Many hardware architectures which use irreversible logic has been proposed for digit-by-digit technique. Array-based arithmetic[6] computation can also be able to reduce power. In calculating square root in,[7] the design of hardware realization of non-restoring algorithm will be done by reversible logic.

The power obtained was high. Computation of Square root requires many reversible logic circuits.

In restoring method, the circuit adds the divisor back and put "0" as the circuit's next quotient digit. Whereas in the non-restoring process, there is no mechanism like that. So, the negative remainder and the number "01" are added and radically right things by a supplementary addition later.

A significant part of the existing algorithms, such as BDD based realization, Positive Polarity Reed Mullerare, is restricted to small and medium process though optimized in gate counts and information bits. In contrast, some realization methods succeed in addressing large functions but expensive in terms of additional gate lines, gate counts and quantum price, mainly from the specifications of irreversible logic. Moreover, exceptional work has done towards realizing the essential reversible computation units like adders, subtractors and multipliers by obtaining a straight translation from traditional to reversible forms. Square-root is most valuable and vital in scientific calculations next to fundamental mathematical operations, i.e. addition, subtraction, multiplication and division. For instance, statistical analysis, complex number calculations, logical analysis, machine graphics and visuals, and signal processing are among the fields where the square root operation is related. Although the understanding of a square root in traditional circuits is well organized. 8- bit binary square root network is a model of square root operation, not a stable structure or generalized approach of creating a reversible square root network. This paper proposes a structured approach for performing the computation circuit. The generation of the reversible embedding, which is an array arrangement of primary blocks, and can apprehend square root networks of any length. To be precise, the standard non-restoring array arrangement of square-root circuit, which operates 2's Complement subtraction regulated by the result of digit-by-digit square root. The proposed design has a reversible controlled subtractor multiplexer(RCSM) block, which produces 2's Complement calculation, and applied in a modular technique to perform the operation of square root.

In Newton-Raphson's method or Heron's method, the solution of square root of a given number is calculated using the formula:

$$x(k+1)=(1/2)(xk+(a/xk)) \quad (1)$$

where "a" is a number, whose square root value will be calculated and xk is iterative

Proposed Models

Digit by digit procedure is used for obtaining a particular binary number's derived square root. Restoring algorithm and non-restoring algorithm are classified from digit G-by-digit procedure. The system's total power is high using the restoring algorithm because it involves a more significant number of hardware resources. When compared to restoring algorithm, the non-restoring algorithm involves a smaller number of hardware resources. The total number of bits N is divided into a group of two digits in the non-restoring algorithm. Therefore, the length of the Quotient is N/2. Steps involving in the non-restoring algorithm are as follows:

- **Step 1:** Separation of the total bits of N into two parts.
- **Step 2:** From the leftmost group of significant bits we have to subtract '1'. If the subtraction will be positive, then Quotient will be 1, then if the difference will be negative, then the Quotient is 0.
- **Step 3:** From the next group of two digits, subtract after appending the previous quotient along with "01".
- **Step 4:** Until we reach till the last of groups of two digits we have to proceed to step -2.

It can be a whole number or radical number in case of radicand. Let us assume that it will be a decimal number, then it will be denoted like 0010.001…And if the radicand is going to be a whole number, then it will be denoted as 1101. In this, 0010 will be linked to 6 and 0011 will be pointed to 0.4 in terms of binary sign. On the basis of requirement the number of bits which are obtained after the decimal point will be prolonged to N that is the total number of bits.

Lets consider a binary square rooter (N7 N6 N5 N4. N3 N2 N1 N0). In Quotient for square rooter it will be going to be (U3 U2. U1 U0). The user can decide the number of bits previously and succeeding the decimal point. For example, the square root of 1101 and 0010.0011 is given in Fig.1.

From Fig. 1, the square root of 13 and 2.2 are found. Value for the square root obtained form 13 will be 3.6. From the quotient 11.10(U3 U2. U1 U0),11(U3U2) corresponds to 3 and 10 (U1U0) to 0.6. The representation of 0.6 in the binary system is 1001.Value obtained for the square root of 2.2(0010.0011) will be 1.4. And the value of the Quotient 01.01, 01(U3U2) will be represented to 1 and 01 (U1U0) to 0.4. The representation of 0.4 in the binary system is

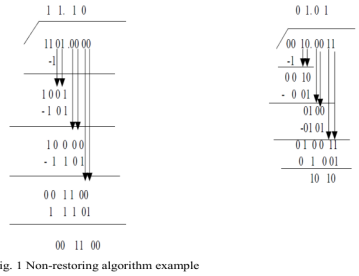


Fig. 1 Non-restoring algorithm example

Fig. 1: Non-Restoring Algorithm

0110. As mentioned, application and user requirement will be deciding count of bits previously and after the decimal point. If there will be a large number of requirement in significant number of bits in the Quotient, then the user shall increases bit size after the decimal point to fulfil the requirement.

A reversible full subtractor is required for computation process which will be done by non-restoring algorithm. The gates like Feynman Gate and Saimur Rahman gate will be designing the square rooter. a full subtractor will be the serviceability of the Saimur Rahman gate. It is clearly presented in the Fig. 1.

Saimur Rahman Gate

A Three bit (3-bit) subtractor is called a Full subtractor. It has 3 inputs, W1, W2, W3 and another input, W4=0 and two outputs difference as W8 and borrows as W7. The mathematical expressions for difference and borrow are

- Difference (W8) =W1-W2-W3
- Borrow W7=1 if W1<(W2-W3) else W7=0

The logical expressions for difference and borrow are

- Difference (W8) = W1 ▫ W2 ▫ W3 ▫ W4
- Borrow W7=W1'W2▫W1'W3⊕W2W3

where ⊕ is Logical XOR operation and W1 'represents compliment operation of W1.

Only in the case of W4=0, a full subtractor will be used which comes from the SRG gate, and also in case of W4 is not equal to 0, in that case, the gate will not be able to work as full subtractor. Garbage output will be represented by W5 and W6. Table.1 will be representing the truth table of SR gate. The radicands (N_7 N_6 N_5 N_4. N_3 N_2 N_1 N_0). with a total length of 8 binary bits. the number of binary bits for the Quotient is half of 8 in the essence of 8/2= 4(U_3 U_2. U_1 U_0) 8-bit square rooter. FG and SR gates will be implemented with the 8-bit square rooter.

Reversible Multiplexer

A multiplexer allows many incoming signals to interact with one device, circuit or resource. Multiplexers also used for the implementation of multiple variable's Boolean functions. The realization of a Multiplexer using reversible logic gates is called a Reversible multiplexer. The proposed design has RT reversible logic gate multiplexer.

If the remainder will be taken as positive, and then the Quotient, i.e. U=1 and the difference will be carried over for the following according to non-restoring computation. But in case if the remainder is taken as negative, then the Quotient will be (U=0), and the previous inputs will then be carried for the following procedure, By using RT reversible gate, a control unit is designed to interchange between the inputs(W1) and the difference(W1). The input(W1), the difference (W8) and the Quotient will given as input to the

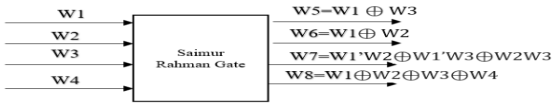


Fig. 2 Saimur Rahman Gate

Fig. 2: SRG Gate

Table 1: Samiur Rahman Gate (SRG) Truth Table

W_1	W_2	W_3	W_4	W_7	W_8
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	0	0	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

gates. For the process of switching among the inputs and the difference we use reversible multiplex.

Based on the Quotient we can be able to see the configuration which is shown in Fig. 3. The difference and the input will be auto switched. Non-restoring algorithm will be proposed by the design with the help of these reversible gates. The basic logic gates OR,XOR,NOT,AND being applied to the traditional approach. We use irreversible gates for the administration of the conventional design. We can finally obtain the power outcomes of conventional and reversible designs.

Working of Square root

Figure 3 depicts that the square root of a binary number can be observed with the help of the Modified Non-restoring algorithm by using the digit-by-digit approach. By using the modified non-restoring algorithm, the provided binary digit is primarily separated into collections of two numbers. Soon "1" is deducted from the left-most significant digits (N7 N6), being the initial step. Next, if the deducted number is zero or greater than zero, the quotient(U3) is regarded as "1", and the RT reversible multiplexer transfers the variation value received of the gate essentially "d" bits (D1D2…) to the next step. Where (D1D2…) are difference bits

If the subtracted value is less than zero, i.e. negative, the quotient(U3) is regarded as "0". The reversible multiplexer transfers the former input data bit to the following step; along with the value received of the previous level, the next couple of bits are considered simultaneously with that value. Those values were saved as "A" bits (A1A2A3…).

The quotient from the preceding step and "01" is added and stocked as B bits (B1B2…), and B bits are deducted from A bits, and this process is iterated till all the digits are finished. The Square root of the provided binary number

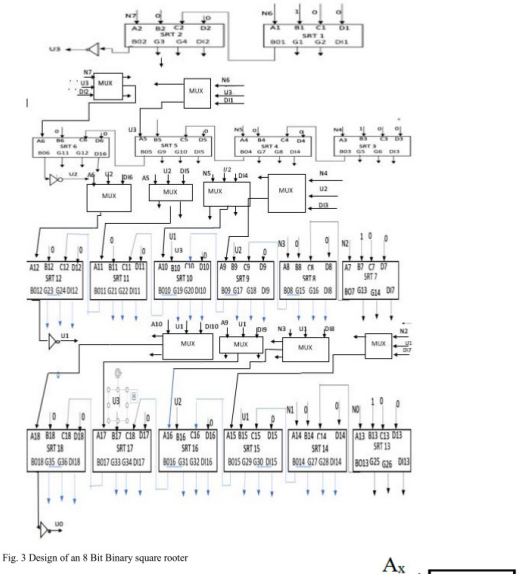


Fig. 3 Design of an 8 Bit Binary square rooter

Fig. 3: 8-bit Binary Square Root

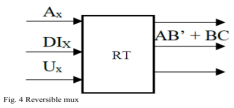


Fig. 4 Reversible mux

Fig. 4: RT Multiplexer

is the terminal quotient, which is the input provided by the user to the circuit. The additional outputs are garbage outputs(G1G2…).

Therefore, using reversible gates such as RT reversible multiplexer, Samiur Rahman Gate (SRG) works as a multiplexer and full subtractor, respectively, by following the Non-restoring algorithm, the square root of a binary number is obtained.

Experimental Findings And Results Of Simulation

Comparison with other methods

VHDL language has been used for coding of the proposed design. Verification of outputs received from respective inputs are processed. If the input radicand is 36, the Quotient is 6, it is observed that from the simulation results shown in Fig4.1. As soon as the design which is proposed will be compiled, the power result is obtained using 90nm technology that is Synopsys Design Compiler for reversible design. From Fig.4.1, Fig. 7 and Table. II we can observe the power and area derived.

Table 2 shows the comparison between the Conventional model and SRG reversible logic model. After Comparing the two models independently, Reversible Logic (SRG) demands fewer logic gates than the Conventional reversible logic based on the non-restoring algorithm for developing the solution for square root.

Table 2: Power Analysis

Approach/Methodology	Algorithm	Gate Count	Power
Reversible Logic (Samiur Rahman Gate)	Non-restoring algorithm	35	65.26 µw
Conventional Logic	Non-restoring algorithm	75	81.65 µw

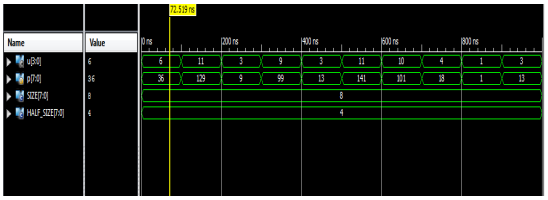


Fig. 5: Simulation output

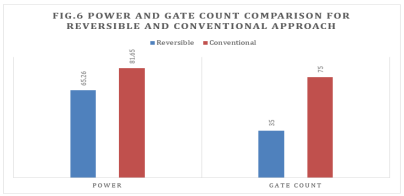
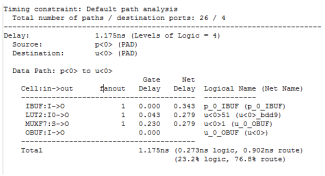


Fig. 6: Reversible logic and Conventional logic comparison

Table 3: Design summary

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	6	204000	0%
Number of fully used LUT-FF pairs	0	6	0%
Number of bonded IOBs	12	600	2%



```
Timing constraint: Default path analysis
  Total number of paths / destination ports: 26 / 4
-------------------------------------------------------------------------
Delay:               1.175ns (Levels of Logic = 4)
  Source:            p<0> (PAD)
  Destination:       uc0> (PAD)

  Data Path: p<0> to uc0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1    0.000   0.343  p_0_IBUF (p_0_IBUF)
     LUT2:I0->O            1    0.043   0.279  uc0>51 (uc0>_bdd9)
     MUXF7:S->O            1    0.230   0.279  uc0>1 (u_0_OBUF)
     OBUF:I->O                  0.000          u_0_OBUF (uc0>)
    ----------------------------------------
    Total                      1.175ns (0.273ns logic, 0.902ns route)
                                       (23.2% logic, 76.8% route)
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Fig. 7: Time summary

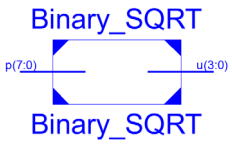

Fig. 8: Binary Square root unit

Xilinx Software will be responsible for carrying out simulations and Synopsys Design Compiler will be the factor for obtaining power. The gate count which has been 75 will be decreased to 35. There will be an improvement of 20% in terms of power.

The Reversible logic RSG model utilizes 65.26 microwatts of power to complete the operation of the square root by measuring the power consumption by the proposed RSG reversible logic model. In contrast, the existing model utilized 81.65 microwatts of power, a

20.0735 change in percentage. Hence, by implementing the energy-efficient binary square root by a non-restoring reversible logic, 20 per cent of power(energy or electricity) is conserved.

The above Design summary table gives information regarding the device utilization on basis of their utilization percentage and their availability of LUT's, LUT-FF pairs and bonded IOB'S.

Time summary of the project shows the timing constraints, total number of paths are 26, destination ports are 4 with 1.175 ns delay. In the time summary delays of each unit and entire model with their gate delays and net delays are represented.

Applications

Various fields have applications based on Reversible logic design, including optical computing, Quantum computing, Quantum Computing Automata, Nano-computing. The research of measurable targets termed as Abstract tools and the computational obstacles that can be resolved using Quantum Computing is Quantum Computing Automata. Other applications of reversible logic design are ultra-low-energy-efficient Very Large Scale Integration(VLSI) designing, Quantum Dot Cellular Automation. An alternative for the limitations of Moore's law on the expectation of computer chip designing; is to formulate quantum chips with the help of reversible logic design. Our ultimate research problem is planning a modern reversible gate, including the implementation towards the perfect Quantum processor that is competent in working with barely energy-efficient computing. It also looks forward in working with high-speeds.

Implementation of an energy-efficient binary square rooter using Reversible logic by applying the non-restoring algorithm can be used for Statistical Analysis purposes, Complex Number Calculations, Logical Analysis of digital machines, Machine Graphics, Signal Processing through the digital binary method.

Conclusion

Binary square root using SRG reversible logic implementation was designed, and the Proposed model and existing model properties are compared. Binary Square root implementation based on a non-restoring algorithm provides the solution with less number of gates and energy efficiency. Resolutions of the proposed model are very adaptable. Minor changes in VHDL code can accomplish the demands of extending the number of bits and number of decimal places after the floating-point. The approaches such as conventional approach and SRG are used for designing the binary square rooter and it will be completed using non-restoring algorithm. Xilinx Software will be responsible for carrying out simulations and Synopsys Design Compiler will be the factor for obtaining power. The gate count which has been 75 will be decreased to 35. There will be an improvement of 20% in terms of power which will be obtained in this paper. Hardware will be consumed less in the non-restoring process, when compared to restoring practice. So thereby, Square root will select non-restoring process. Thus, with all the necessary parameters an energy efficient reversible binary square rooter was successfully implemented. ALUs will be using square rooter for reversible computing especially for reversible computing. There will be a decrease in the gate count and also the conventional approach will be consuming more power when compared with reversible computing.

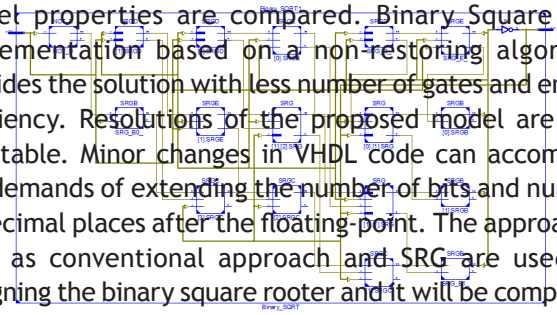

Fig. 9. Reversible Logic Binary Square root circuit by non-restoring algorithm

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