Journal of VLSI Circuits and Systems, ISSN: 2582-1458 Vol. 5, No. 2, 2023 (pp. 8-14)

RESEARCH ARTICLE WWW.VLSIJOURNAL.COM

Digital Filter based Adder Module Realization High-Speed Switching Functions

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KEYWORDS:
Adaptive FIR filter;
Carry-save adder;
Distributed Arithmetic;
LUT;
Ripple carry adder.

ARTICLE HISTORY:
Received 10.07.2022
Accepted 15.08.2022
Published 27.09.2022

DOI:
https://doi.org/10.31838/jvcs/05.02.02

Abstract

FIR filter bank play a vital role in any signal processing systems. The FIR filter is used to implement any frequency response digitally. Usually, the FIR filters contain multipliers, adders and many delays. As we know, the number of MAC operations (multiply and accumulate) makes the FIR filter less efficient and increases hardware complexity. So in this project, we included DA (Distributed Arithmetic) architecture in designing the efficient adaptive FIR filter. The pipelined Distributive Arithmetic architecture provides less power, less area and high values of throughput in creating an adaptive FIR filter. These are used in Echo cancellations, Radio channel equalizers and speech coding. DA architecture also helps in improving the processing speed of the FIR filter by eliminating the number of multipliers. A reconfigurable filter design can be achieved with the help of this Distributive Arithmetic architecture. Here the sum of the partial products which is pipelined is passed as the input values, and it is stored in the LUT (lookup tables) of the distributive architecture. By replacing the adder of the shift accumulation unit with a carry-save adder, the area of the proposed design is reduced. By placing the ripple carry adder, the size and delay are reduced to a further extent. Here we will use the Xilinx ISE tool to verify the simulation result, area required and time consumed.

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How to cite this article: Al-Yateem N, Ismail L, Ahmad M. Digital Filter based Adder Module Realization High-Speed Switching Functions. Journal of Complementary Research, Vol. 5, No. 2, 2023 (pp. 8-14).

Introduction

Filtering is required to enhance, adjust, or modify digital signal processing (DSP). They help in removing the noise from the signals.[1-15] The Adaptive FIR filters are one of them, which are used in many signal applications. These filters are commonly used in image processing to enhance the image or restore the data by significantly removing noise. This adaptive filter keeps on updating the filter values as it proceeds. It tries to remove or minimize the error between the input and the output by finding the difference between the musing error functions. These filters provide the linear model, inverse model of the unknown system and predict the present value of the random signal.[16-25] They can be designed as FIR or IIR filters. The adaptive FIR is more preferred because of its stability and easy updating of the filter coefficients.

The adaptive filter is used in systems that deal with random statistics, for example, noise. In many applications such as telecommunications, radars, sonar, audio signals etc., an adaptive filter can cancel or equalize noise. The basic understanding of Adaptive filters is they try to equalize the random noise; if it can't equalize, they try to track the random statistics.[26-35] As noise is randomly occurred the coefficients change randomly, which results in increased complexity of the task for the filters. Some of the commonly used Adaptive filters are LMS and RLS. The LMS adaptive filters are preferred because of their system stability. LMS has a simple design and good convergence performance when compared to RLS.[36-43] [36]-[43].

The Finite Impulse Response is a digital filter that is the most frequently used component in many signal and image processing applications. FIR filter, which has the minimum time delay, gives a better response when compared with others. Area utilization and time delay are two crucial

factors for designing any filter. By determining suitable architecture, these factors can be reduced.[44]

Adaptive filters are usually designed and implemented using multipliers, memories and adders. The adaptive filters have more hardware complexity because the multipliers take more area and power. We can reduce this complexity by designing it in multiplier-less architectures. So we can use Distributed arithmetic architecture which is a multiplier-less design architecture used to reduce the hardware complexity because of its area efficiency and less computing time. It is used to calculate the sum of products and occupies less area in many DSP applications when the order of filter increases. Distributive Architecture can compute using the bit-serial operation. Here lookup table (LUT) is used for updating the coefficients and performs the shifting operation to get the output calculations. High throughput is achieved by LUT because it is used in filtering and weight updating operations.

The filter structure is shown in Fig. 1. It estimates the error and the output for every cycle.

The Input signal X (n) is given as

$$X(n) = [x(n), x(n-1) \ldots x(n-N+1)]T \quad (1)$$

X(n) is the input sample signal given time 'k' and the vector 'T' transpose.

The output Y(n) is

$$Y(n) = XT(n)\, r(n) \quad (2)$$

Where r (n) is the coefficient of the filter vector and is represented as

$$R(n) = [r0(n), r1(n), r2(n), \ldots, r(N-1)(n)]T \quad (3)$$

The LMS algorithm for weight updating according to Windrow is

$$R(n+1) = r(n) + \mu(e(n)X(n)) \quad (4)$$

Where e(n) is the error signal, μ is a parameter for step size, which is used to determine the speed and accuracy. The error is obtained by the estimated by subtracting the required signal and the obtained signal.[45-49]

The equation can be given as

$$E(n) = R(n) - Y(n) \quad (5)$$

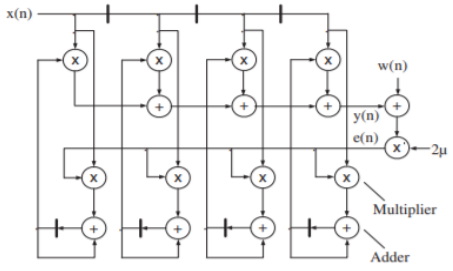

Fig.1: Basic adaptive filter

where R(n) is the required signal. For every sampling period, the filter input signal X(n) is fed to the delay, and then it is shifted to its right.

In regular FIR filters, the size of the filter increases with an increase in multiplexers, adders, coefficients and delay elements. For instance, a four tap filter requires four multiplexers, three adders, three delay elements with four filter coefficients. But with a DA-based FIR filter requires only one adder and no multipliers. The operation speed improves, and power consumption decreases, and, most importantly, a vast area is saved.[50-59]

Here, we discuss the DA-based adaptive filter with less delay and less power usage. It is greatly reduced to a larger extend by removing. The resultant throughput rate is high due to using a carry-save accumulator. The carry-save accumulator is replaced in place of the shift accumulator.Carry save adder is used to reduce the no. of inner multiplications of the sampling period. By using LUT, Carry save adders and eliminating multipliers, a substantial amount of area is saved, and High Throughput is achieved. The operations are performed by using the shift and add principle. Further, by replacing by a ripple carry adder, the efficiency is increased.

The rest of the paper contains the following. In the further section, we will discuss the adaptive filter using DA. The detailed design process of Distributed Arithmetic adaptive filter with pipelined structure is discussed. Further, the proposed DA-based adaptive filter with carry-save adder and ripple carry adder—next, the obtained synthesis outputs of the existing architectures and proposed design in Xilinx ISE tool. Finally, conclusions are given.

Proposed Models

The proposed provides a Reconfigurable FIR Filter design on the Distributed Arithmetic algorithm. It contains a feature of reconfigurability in terms of its hardware. This feature provides the flexibility to use this design in a wide range of filter coefficients which can even change at the runtime. The efficiency of the mechanism is improved by using the distributed architecture. We can make different modifications to this architecture for improved performance. When the inner product computations are dominated, we use this DA architecture. This architecture has more area and power benefits. We must seriously consider DA architecture if the performance to cost ratio is critical. Herewith the increase in the number of filter coefficients, the need of changing the hardware configuration of the circuit is eliminated as it is flexible. The FIR filter implemented in this design architecture may be applied to any filtering application in a communication system.

Distributive Arithmetic (DA) LMS adaptive filter

A standard digital system will require K multiply and accumulate (MAC) operations in its design. The

operation must be faster for larger K values. It is a major limitation for the system.[34] Hence we use the distributive arithmetic architecture, in which the operation is done in bit-serial fashion. In this architecture, the standard multipliers are replaced by the memories and the adders. It has an efficient mechanism in its operation. It is also suitable for time-varying coefficient vectors. This type of architecture is implemented to generate the inner product multiplication and vector to vector multiplication in limited operations. Arithmetic DA gives faster results and higher throughput. This type of implementation is an attractive option in the digital system.[43]

The DA based adaptive filter structure provided with N = 4 length is as shown in above Fig. 2. It has a majorly five important blocks; they are 4-point inner prod-uct block which is the important block. Next, we have the weight updating block for updating the resultant or obtained weights to it, control unit block where all control operations are performed, error calculation to find the error and sign-magnitude controller units for the sign of the coefficients. The above block of the four-point inner product has the Distributive Arithmetic table, MUX, XOR, and the carry-save accumulator, which perform the shift accumulation. In the carry-save accumulator, the weight vector is given in order of LSB to MSB one after the other. The bit slices are usually given the 2's complement form in the MSB. Hence all the lookup tables are fed to the XOR gates along with the sign because the output is also in the 2's complement form. In the last, all the outputs from the XOR gates are added, and the final output is calculated.

The Distributive Arithmetic table has 16 memory units such as registers, which can store up to sixteen combinations

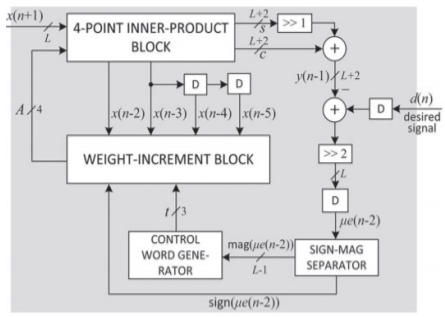

Fig. 2: Distributive Arithmetic (DA) LMS adaptive filter

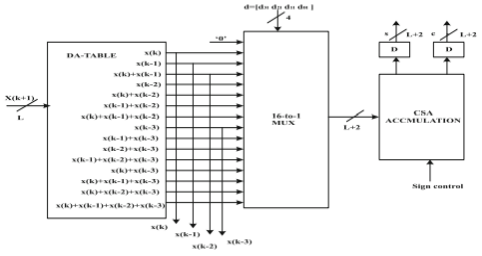

Fig. 3: Four-Point inner product block

of inner product data, and it is passed as the input to the 16:1 multiplexer. The 16: 1 multiplexer (MUX) to select the values from the registers. The filter coefficients due to the feedback from the weight updating block will be given as the selection lines to the MUX, and the result which comes from the MUX is fed to the unit of the accumulator. For sign control, the outputs of MUX are fed to the XOR. Using the fast bit clock cycle to the accumulator of the carry-save adder, which gives sum and carries, we get a high throughput rate. The sum and carry are generated, and they are added to get the resultant filter result y(n). The output y(n) is then removed from the required signal denoted as R(n) to estimate the error value e(n) of the filter.

In the next block, we have a main block called weight increment which contains 4 barrel shifters that performs the shifting operation, four adders or the subtract and a bit-serial converter in the parallel design. With the barrel shifter, we multiply the input signal x(n), and error e(n) is done. This obtained updated weight is produced by adding or subtracting with its current weight. These weights are updated than are fed as the selection lines to 16:1 MUX to the inner product unit.

Pipelined Distributive Arithmetic based adaptive FIR filter

FIR filter is used in many digital signal processing applications. They are used in noise cancellation, equalization, speech processing and many different types of applications. Many of these applications require an FIR filter of higher-order, which contains a huge of multipliers and adders, which decreases the efficiency and performance of the system. The power and delay is more due to these memory blocks. Several design architectures are realized for the efficient use of these FIR filters by using the Distributive arithmetic architecture and multiple constant multiplication (MCM) architecture.

The DA based architecture uses the LUT, which are called lookup tables which are used to store the pre-calculated values in it to reduce the complexity in the design. On the other hand, the MCM is used to reduce the number of additional operations performed. In the basic DA based architecture, it uses bit-serial operation; hence we can observe there increase in the delay because here, all the values or coefficients are stored in a single LUT. So we use parallel DA architecture. In Parallel DA architecture, instead of storing these values in a single LUT, it gets split into several ROM LUT's. In this, it performs a parallel mechanism that is all the LUT's are provided with different inputs at the same time; thus, it increases the speed of the operations; hence we can observe the efficiency in the time consumed.

But this structure has a limitation that is the data stored in ROM cannot be altered. So it is improvised with

a split LUT and some change in the design. Instead of ROM for each input, LUT is given with a set of 4 data's which is also a parallel operation. It is a flexible design structure. The limitations of this structure are, as the no. of inputs gets increased, similarly there an increase in the LUT, thus resulting in an increase in hardware usage. We use the pipelined distributive arithmetic architecture to remove these drawbacks and limitations: In this Distributive Arithmetic based adaptive FIR filter, initially, the inner products are calculated using the DA table, which contains memories and the adder circuit. The method while designing the filter depends upon the implementation and its specifications. In distributive architecture, we use LUTs. LUT simple generates the output based on the input. The LUT(Look-Up Tables) to used store to store the pre-computed values of filter coefficient for further required operations. These are basically used for filtering and to update the weight but, it is mostly suitable for lower orders.

The inner product of the DA table is shown in Fig. 4. Here the x (n + 1) is given as input with the desired length here, we denoted as L is passed to the memory block, and we get the output as x(n). Next, this x(n) is then fed

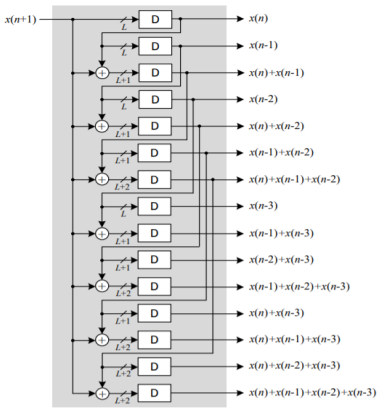

Fig. 4: Distributive Arithmetic table to get the sum of input samples

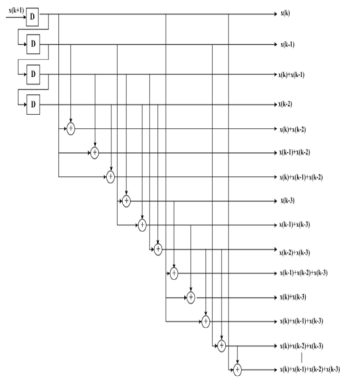

Fig. 5: DA table for the pipelined Distributive Arithmetic FIR Filter

to the memory block to get the x(n – 1) values. Now, the input values which are x(n + 1) and x(n) are added and fed to the memory block to get x(n) + x(n – 1). In the same manner, we get the outputs which are represented as x (n – 2), x (n) + x (n – 2), x (n – 1) + x (n– 2)..., and continues and finally, these results are fed as input values to the 16:1 MUX as the selection lines.

The DA table output requires 15 registers and seven adders for its implementation. These registers take up more area and also consume huge power during its operation. To remove this limitation, we implemented a pipelined DA table, as given in Fig. 5.

For the DA table (Fig. 5) design, rather than passing the x(n + 1) input values to the adders and memories, we fed the previously obtained register samples as feedback to the input values to the adder to get similar properties. With its implementation, the DA table's inner product is obtained with four delays and ten adders. Thus reducing the table to eleven registers. Here, we the pipelining concept by using the delay elements. It helps to develop the overall speed of the system. The adders are increased to three. By implementing this proposed structure, the area of the DA-based adaptive filter can be greatly reduced. The adders in the above circuit can be replaced by the carry-save adder to reduce the area and decrease the computational time.

The carry-save adder has faster addition logic and reduces the propagation time or delay in the system. We can also use the ripple carry adder for better efficiency. In the proposed architecture, the no. of registered users is reduced so, the speed and the performance increases. The proposed design executes more no. of outputs for each cycle when it is estimated with the existing designs structures. The area utilized by the proposed DA architecture is very minimum it is when compared with the proposed design architecture.

Simulation Results

Existing Method using CSA

The performance of the proposed architectures has been substantially validated through their implementations on

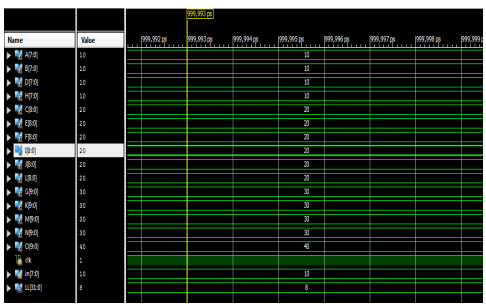

Fig. 6: Simulation output of existing model using CSA

Table 1: Comparative Validation of Proposed Model With Existing Standard Designs Using CSA and RSA

Parameters	*Existing Model Using Csa*	*Existing Model Using Rca*	*Proposed Model Using Csa*	*Proposed Model Using Rca*
No. of the slice registers	203	38	38	35
No. of slice LUT's	242	249	249	172
No. of fully used LUT-FF pairs	138	32	32	32
No. of bonded IOBs	145	1 45	145	145
No. of BUFS/BUFGCTRLs	1	1	1	1
Time delay	4.239ns	1.393ns	1.393ns	0.543ns

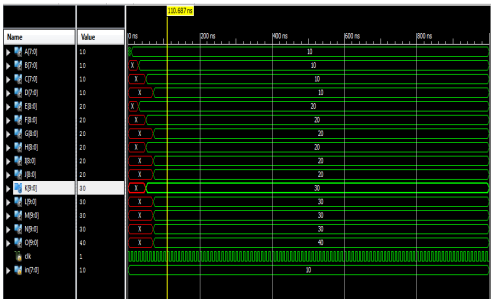

Fig. 7: Simulation output of proposed model using CSA.

the Xilinx platform. A detailed comparison of the design metrics with the existing methods is also presented. If the performance to cost ratio is critical then, then it is preferred to use the DA architecture. It is mostly recommended when the inner product computations are dominant.

Proposed Method using CSA

The results exhibit the important characteristics of architecture given their performance and the selection of a better architecture for an application based on the modern digital technology era requirements Fig. 7).

Validation of the Proposed Models

Table 1 shows the comparison between the existing model using CSA and the existing model using RCA, and we can observe using RCA is more efficient in many parameters. Similarly, we can observe the comparison between CSA and RCA using the proposed model. These both are more efficient when compared with the existing models.

Conclusion

We have implemented the pipelined Distributive Arithmetic based adaptive FIR filter for the low area, large throughput, and less power using the carry-save adder and ripple carry adder. The faster clock pulse is passed to the carry-save adder present in the accumulator unit; then, the throughput value is increased. It can be replaced by a ripple carry adder for better efficiency. A-based FIR filter with the carry-save adder and a modified left shift accumulator is developed, giving a higher speed and significant reduction in the area. For high-speed applications, the carry-save adders are considered a better choice than using the ripple carry adder. The proposed architecture has 14% less in power and 30% less in area when compared to the existing model.

The Distributed Arithmetic (DA) based method is more preferable since it removes the purpose of the large hardware multipliers and is able to execute large filters with a high throughput rate. The most widely used design metrics to quantify the performance of an FIR filter are high throughput/speed (maximum frequency), area (occupied slices), Latency (clock cycles), and power (milliwatts). In this dissertation, an earnest effort has been made to design FIR filter architectures using DA with the goal of minimizing the area delay complexity and improve efficiency. The modified shift accumulator composed of pipelined bit-serial adders such as carry-save adder, ripple carry adder reduces the critical path, thereby yielding a higher speed of operation with a small escalation in the number of occupied slices. This research work is further extended to develop a new architecture for a high-speed FIR filter, with linear rows of processing elements and a new pipelined shift accumulator tree that results in low latency and fewer hardware resources.

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