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Universal Shift Register: QCA based Novel Technique for Memory Storage Modules

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Abstract

A Quantum-dot cellular automaton (QCA) represents a modern technology for implementing small-sized circuits with high-performance, low-power consumption and various computations in digital circuits at the nanoscale level. These quantum dots made up at a nanoscale level which increases the performance of circuits. With the invention of QCA in electronics, the circuits can achieve their operations with very high efficiency and with low power dissipation. Meanwhile, a universal shift register (USR) is a particular circuit with the functions of storing and shifting bits to a specified direction and is observed as an essential component. This USR also has the process to load the data. Therefore, here we propose a USR circuit based on QCA, i.e., QUSR, which requires the essential components of a shift register and a multiplexer (Mux) combined and used to select the operation of the USR. In this project, we propose a 2-to-1 Mux, which then extended to a 4-to-1 Mux. Here, we suggest a new D flip-flop and design a shift register by connecting all of these. Finally, we propose a QUSR that consumes low power and computes high-performance by combining four 4-to-1 Muxes and a four-bit shift register. The proposed QUSR is highly efficient in time and space complexities and has a good energy dissipation performance. The proposed design performance metric of efficiency achieved by doing required simulations using the QCA Designer tool.

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Introduction

According to Moore's law, the count of transistors and other electronic components on the chip are rapidly increasing using very large-scale integration (VLSI) technology. As a result, it is that much not easy to increase further the count of electronic components in establishing VLSI components. Since more electronic components may increase the size of the chip and increase the temperature inside the chip, that results in damage to the chip.[1-12]

The QCA performs highly dense computing, realized in various material systems; thus, it becomes an alternative to VLSI. In conventional digital systems, the information is transferred from one place to other through electrical current, while in QCA, cells transmit information by propagating a polarization state. So, we introduced QCA technology; in this technology, quantum dots intended to replace the traditional transistor technology, which continues to occupy massive space despite continuous breakthroughs in VLSI technology. The minimization of power dissipation has also entered a stalemate. Hence it is imperative to search for their alternative QCA technology introduced into the picture to establish USR with four D flip-flops and four 4 to 1 Mux connected, as shown in fig1. We Implemented and evaluated this USR in parallel-in-parallel-out mode and verified the results.[13-28]

About QCA

Quantum-dot Cellular Automata (QCA) is a nano technology that John Von Neumann introduced. It consists of a uniform grid of cells, and each consists of four dots assigned with Quantum Dots and electrons together. There are two states named +1 and -1 (Logic 1 and Logic 0). This uniform grid of cells connected in a series called an "Array of cells" or "Quantum wire" transmits an equal amount of energy from beginning to end.[29-37]

As propagating through cells, the state logic of each cell logic carried to the next adjacent cell in a row. If it passes as diagonal, then it changes its state to +1 to -1 or vice versa. To implement this QUSR, we have QCA Designer Tool software in which at first we implemented basic gates (optional), D flip-flop, and 2 to 1 Mux. The 2 to 1 Mux then extended to 4 to 1 Mux. Moreover, by making a copy of each of the circuit four times, the connection is made. Then, we had implemented our project 4-bit QUSR model, and the results are verified.

Furthermore, the tool also contains four clock signals to give better results as outcomes—the phase of the fourth pulse changes opposite to the first clock pulse. Moreover, it includes two simulation engine types, namely Bistable Approximation Simulation and Coherence Vector Simulation (Fig. 2).

BASIC GATES

Basic gates such as "AND" gate, "OR" gate, "NOT" gate are designed and implemented using QCA Designer Tool.

AND gate (Table 1 and Fig. 3):

$$OUT = A.B \quad (1)$$

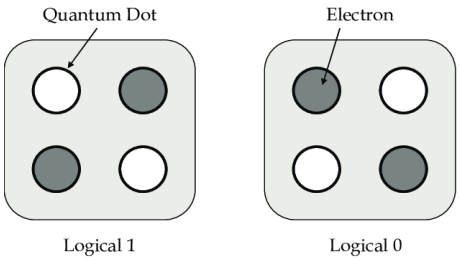

Fig. 1: Basic QCA cell

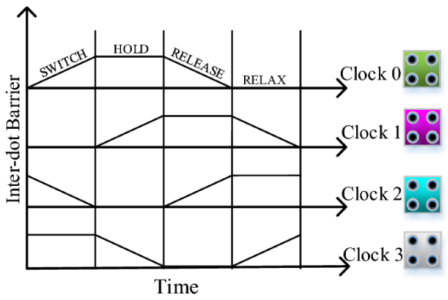

Fig. 2: Phases of clock signals in QCA

Table I. Truth table of AND Gate

A	*B*	*OUT*
0	0	0
0	1	0
1	0	0
1	1	1

OR gate (Table 2 and Fig. 4)

$$OUT = A+B \quad (2)$$

NOT gate (Table 3 and Fig. 5)

$$A\_bar = not(A) \quad (3)$$

The above three are basic gates designed and implemented using the QCA Designer tool and verified the simulation results with the following truth tables.

PROPOSED MODELS

Implementation of D Flip-Flop

D flip-flop is a digital electronic circuit, and it used to delay the change of state of its output signal until the next rising edge of a clock timing input signal occurs. The D flip-flop is essential, and it gives the solution when SR inputs have high logic, and the output may be forbidden. Introduction of an inverter in between the inputs of SR flip-flop and allows a single input D to overcome that situation.

The QCA with four clocking zones is used to implement a D flip-flop. The proposed D flip-flop using QCA technology

Fig. 3: AND gate

Table 2. Truth table of OR Gate

A	*B*	*OUT*
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 4: OR gate

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implemented in the QCA Designer tool shown in Figure 7, which produces the equal outputs as basic D flip-flop generates. The parallel input parallel output of QUSR designed using this D flip-flop (Table 4).

The series combination of four D flip-flops used to implement this proposed QUSR. It has four parallel data inputs from D1 to D4 and four similar outputs, Out1 to Out4. When we gave the four inputs and also clocked input simultaneously, the outputs also get simultaneously.

Implementation of 2 to 1 Mux

The multiplexer, in short MUX, is a combinational logic circuit designed to switch one of the several input lines to a single standard output line using the control signal/ select signal. Therefore, the select line acts as a rotary switch when it OFF (logic 0), picks one as output, and when it ON (logic 1), it picks another as output. Therefore, MUX operates like fast-acting multiple position rotatory switches connecting and controlling numerous channels/ input lines.

It consists of two inputs which are I0 and I1, and one select line S, for which the select signal selects the input signal to flow through an output Out, which means the output is connected to any of the inputs depending on the select signal. This circuit mainly used in discrete signals in which, from the specified signal chosen, the outcome connected to selected inputs. That implies at one instant of time, and it selects only one input to flow through output.

The proposed 2 to 1 Mux using QCA technology implemented in the QCA Designer tool shown in Figure 9, which produces the equal outputs as basic 2 to 1 Mux generates.

Table 3: Truth table of AND Gate

A	A_bar
0	1
1	0

Fig. 5: NOT gate

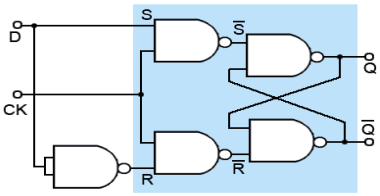

Fig. 6: Basic D flip-flop

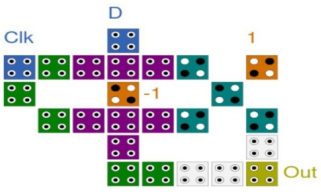

Fig. 8: Proposed D flip-flop

Table IV: D flip-flop truth table

Clk	*D*	*Out*
0	X	Memory
1	0	0
1	1	1

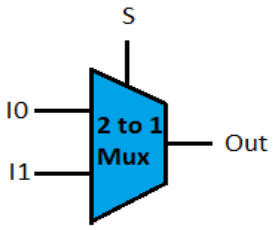

Fig. 9: Basic 2 to 1 Mux block

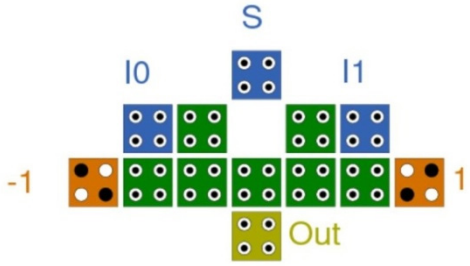

Fig. 10: Proposed 2 to 1 Mux

Table 5: 2 to 1 Mux truth table

S	*Out*
0	I0
1	I1

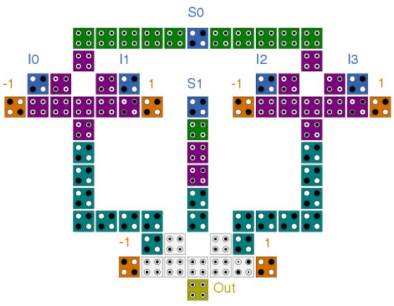

Fig. 11: Proposed 4 to 1 Mux

Implementation of 4 to 1 Mux from 2 to 1 Mux

By using three 2 to 1 mux's, we had designed one 4 to 1 mux. For that, we must require three 2 to 1 mux's to that four inputs and two select signals; based on the selected signals, the output connected to corresponding input signals. In this instance, only one of four inputs is connected to the output, which can be achieved by selected lines S1 and S0 act as a rotatory switch to produce the desired output response. The proposed 4 to 1 mux is shown in fig.10 and verified the results from the truth table given below table 3.

This 4 to 1 mux has two selected lines, namely S1 and S0, which indicates the output to connect for the specified input. Thus, 4 to 1 Mux acts as a four input and one output selector circuit, selecting the required operation to perform in our project.

Implementation of USR

Universal Shift Register (USR) is a register used to store and shift the bits of the data in the required directions with parallel load capability. It can also be used to perform input and output operations in both serial and parallel operations. The unidirectional and bidirectional shift register are combined to get the design of the USR. A USR has both shift-right and shift-left signals; they are used to move the data according to the given input information. When shift left operation is performed, the data transfer shift towards the left in the serial path; similarly, when shift right operation is performed, the data transfer shift towards the right in the serial direction. When parallel load operation is performed, then data stored in parallel and gets output in parallel. Hence the USR can do both input and output operations with both serial and parallel loads. In this project, we are implementing a parallel-in-parallel-out universal shift register. That means we are operating the USR to perform parallel loading and parallel retrieving of the data.

Our proposed USR contains four input signals, one shift-left signal and one shift-right signal; based on the selected signals, the required operation performed. Moreover, it can be used for loading data and retrieving data of concerned clock signals. From the below basic block diagram, we can observe how a USR works.

Table 6: 4 to 1 mux truth table

S1	*S0*	*Out*
0	0	I0
0	1	I1
1	0	I2
1	1	I3

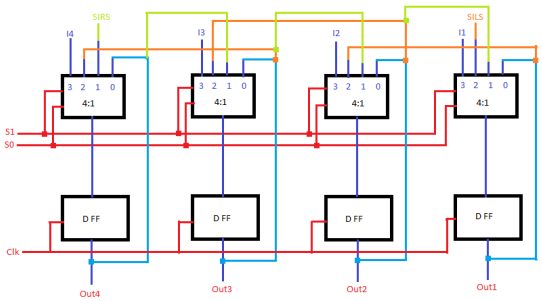

Fig. 12: Block diagram of USR

Operation

When select lines S1 and S0 are logic low, then "0" of each Mux selected as output in Mux that carried to D flip-flop, and it again connected to "0" of the next Mux and continuous. That means the means data is unchanged.

When select line S1 is low, and S2 is high, then "1" of each Mux selected, which means shift right operation performed, the output of every D flip-flop connected to the next Mux. That results in shifting the data in the right direction.

When select line S1 is high, and S2 is low, then "2" of each Mux selected, which means shift left operation performed, the output of every D flip-flop connected to the previous Mux. That results in shifting the data in the left direction.

When select line S1 and S0 are logic high, then "3" of each Mux selected results in parallel loading of data; the same output of each Mux given as input to every D flip-flop. Then the main aim of our project that is parallel-in-parallel-out, is achieved.

The figure 13 is the USR of QCA technology designed using the QCA Designer tool, which performs the

Table 7: USR Operation for specifically selected inputs

S1	*S0*	*Output*
0	0	Unchanged
0	1	Shift-Right
1	0	Shift-Left
1	1	Parallel Load

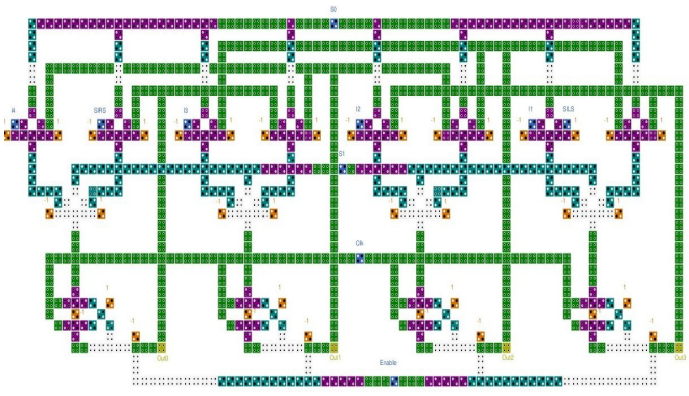

Fig. 13: Proposed USR using QCA Technology in QCA Designer Tool

operations of the primary Universal Shift Register. To load data in parallel-in-parallel-out form, store data, and shift the data by specified direction. In this circuit, enable is always high that clears each flip-flop results and each clock signal. A clock signal deployed to perform memory storage in the flip-flop. S0 and S1 used as selected lines, and this circuit is a four-bit USR, so four inputs are given to "4" of each Mux.

Simulation Results

Figure 13 represents the simulation of a D flip-flop that states when CLK is logic high, and then it gives D has output; else it gives logic low has output. Figure 14 represents a 2 to 1 MUX simulation, which states when select line S handles the input to go through the output. Figure 15 represents a 4 to 1 MUX simulation that states depending on the selected line S1 and S0; the output gets from the given inputs.

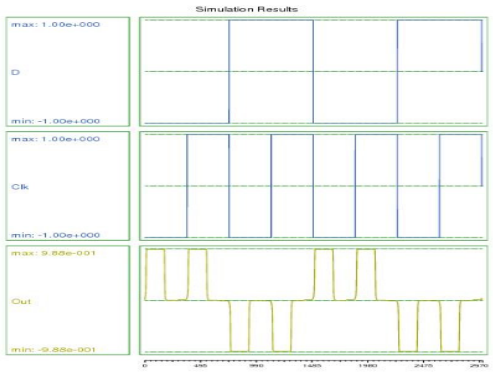

Fig. 14: D Flip-Flop QCA Simulation

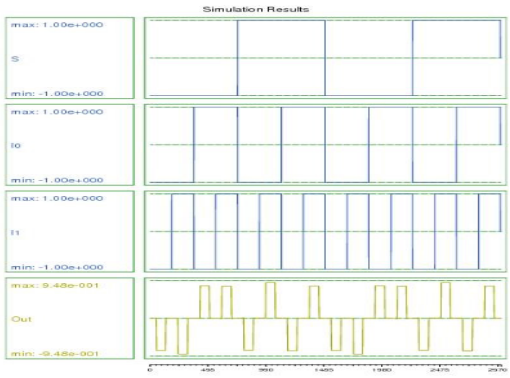

Figure14. Mux 2 to1 QCA Simulation.

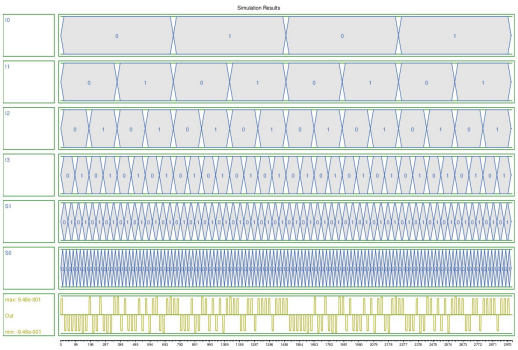

Figure15. Mux 4 to 1 QCA Simulation.

Table 5: Existing vs Proposed model

Case	*Existing Model*	*Proposed Model*
Efficiency	Medium	High
Performance	Slow	Fast
Complexity	Hard	Simple
Power consumption	More	Low

The table 5 states that this proposed model of USR has many advantages compared to the existing model in the field of electronics. The parameters like efficiency, performance increases and complexity and power consumption decrease by using QCA technology. Therefore, USR designed and implemented using the QCA Designer tool application.

Conclusion

The USR designed using QCA technology on the QCA Designer tool to store and shift data in both directions (left and right) using a D flip-flop and 4 to 1 Mux. That helps to minimize power consumption and increase its performance compared with the existing model, VLSI technology. This kind of USR implemented with the help of nanotechnology, and then it evacuates the VLSI in creating chips with transistors and other electronic devices in the design of USR. That can be done when nanotechnology comes into the electronic field; then, many inventions may be made and improve this project and be applied to get product-type results. From the obtained results obtained, we can conclude that by using the QCA Designer tool, we can design USR by using QCA technology and can operate in parallel-in-parallel-out mode and make efficient and has fast response when compared to the VLSI model of USR.

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