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CSA Implementation Using Novel Methodology: RTL Development

Kriti S. Chakma[1], Md. Sarwar U. Chowdhury [2]

[1,2]Department of Electrical and Electronic Engineering, International Islamic University Chittagong, Chittagong 4318, Bangladesh

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Abstract

Carry Select Adder (CSLA) is an essentially utilized adder on account of its higher computational speed. CSLA is utilized in the space of incorporation frameworks. This paper proposes a CSLA design by carrying out the Logic Optimization Technique (ZFCLOT) using Zero Finding Logic contrasted with ordinary Zero Finding Logic (ZFC). This paper notices the different presentation measurements like area, power, delay, area delay product (ADP), power delay product (PDP) and effectiveness. Approval of the ZFCLOT put together CSLA is displayed with respect to Cadence stage utilizing 45 nm platform. The presented CSLA utilizing ZFCLOT has shown advanced execution measurements, explicitly, region and power improvement of 47.287% and 49.1%, separately contrasted with the current standard plans.

Author's e-mail: Chakma.ks@gmail.com, Chowdhury.uds@gmail.com

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Introduction

In the present digitalized world, there is critical significance in planning, acknowledging and carrying out the structures of circuits to perform paired expansion and improve the presentation of different cut off points in computerized signal applications like Processing of signal in digital industry and Processing of signals in biomedical industry. The speed of a particular plan is by and large dictated by the critical path delay (CPD). Ripple carry adder (RCA) is utilized to duplicate full adders which, is executed in a course technique. CPD for such kind of RCA adder restricts the speed of the framework.[1-10]

A carry select adder (CSLA) is utilized to diminish this presentation metric, for example CPD. One of the productive plans to improve the speed of multi-bit adders is Square Root (SQRT)- CSLA.[1] CSLA is planned by utilizing two RCAs, in which each has input carry 0 and 1, separately; as indicated by the forming carry input, the exact whole and carry yield is chosen. The expense of the chip is chosen by the adder plan. Thus, the cost will likewise be diminished when the space of a particular plan is decreased.[11-20] Customary CSLA is quicker than RCA, however quite possibly the most and basic execution measurements, an area that influences the plan cost. The Logic streamlining procedure diminishes the region where rationale is addressed without changing its comparable recurrence. Different Logic enhancements have been performed to diminish an area by utilizing a circuit with an expansion in CPD.[21-28]

To advance the region, in CSLA the Zero Finding Logic (ZFC) is used as the development for the reason to optimize the area.[2] The combinational postponement is expanded due to the utilization of XOR & AND entryways.[29-35] By altering the ripple carry adder for improving region, CSLALOT is planned.[3] However, the speed of the engineering is decreased by the use of countless gatherings. Planned CSLA designs by utilizing circuit improvements and rationale advancement strategies for speed, region and power productivity.[4] All these presentation measurements can't be tended at a time. In this way CSLA is planned by utilizing NAND entryways and additionally entryways to achieve fast.[36-43]

However, the development possesses added region when contrasted with CSLA planned by bit-cut squares. In this paper, CSLA utilizing altered ZFC that is ZFCLOT is designed to diminish the region. The proposed architecture results and correlations are described in Section 4. At last, conclusion is given in Section 5.

Proposed Models

Architecture of Zfclot

The design and construction of CSLA using ZFCLOT are implemented by utilizing the technique of logic optimization. The construction of ZFCLOT of CSLA consists the quantity of eight modules. Table 1 shows the designs utilized in ZFCLOT of CSLA. As the module size rises, extra half adders are required, that in turn decreases the area.[46-58]

Ripple Carry Adder using two full adders (RCA)

This is one of the internal module used in the implementation of CSLA. It comprises of two full adders. The main full adder has three inputs as A0, B0 and Cin. Now, the outputs of first full adder has a sum S0 and a carry C which is taken as one of the input to the second full adder along with A1 and B1. At last, the final outputs obtained are S1 and Cout as shown in Fig. 1.

Ripple Carry Adder with one half adder and full adder (RCA 0)

This is also one of the internal module used in the implementation of CSLA. It consists of one full adder and one half adder. The half adder has two inputs as A0, B0. Here, we consider Cin as 0. Now, the outputs of half adder has a sum S0 and a carry C which is taken as one of the input to the full adder along with A1 and B1. At last, the final outputs obtained are S1 and Cout as shown in Fig. 2.

TABLE 1: Modules used for designing CSLA

Module	*Set 1*	*Set 2*
Module 0	Ripple Carry Adder with carry	-
Module 1 - Module 7	Ripple Carry Adder with 0 carry	ZFCLOT

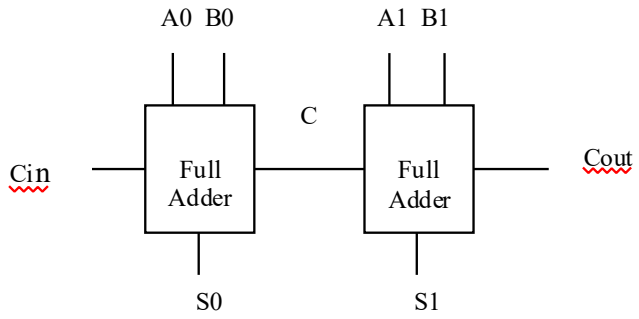


Fig. 1: Ripple Carry Adder using two full adders (RCA)

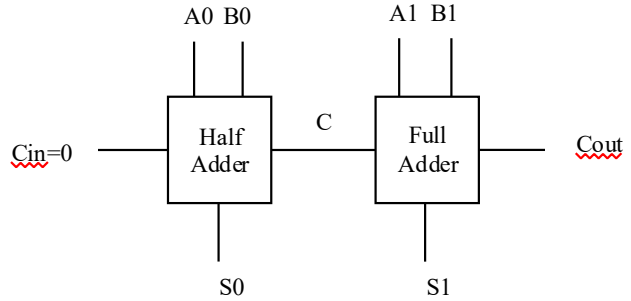


Fig. 2: Ripple Carry Adder with one half adder and full adder (RCA 0)

3 – bit ZFCLOT

Every module has two information inputs. 16-bit information modules are isolated such that each gathering has two information inputs. Alongside the information inputs, each gathering has either input carry cin or carry before carry CP. Module 0 comprises of a 2-cycle RCA. Module 1 to Module 7 comprises of RCA 0 and ZFCLOT. The development for Zero Finding Logic of 3-bit utilizing logic enhancement technique (ZFCLOT) is appeared in fig.3. NAND entryway utilizes low region and furthermore devours less power contrasted with XOR - entryway [6][7]. Subsequently to diminish the region and power utilization, ZFCLOT is planned utilizing NAND entryways. Here, the execution of CSLA utilizing ZFCLOT is animated utilizing the 45 nm Cadence devices. OR AND INVERT (OAI) Logic is used as one of the parts in designing 3 - bit ZFCLOT.

In this logic, the first two inputs which are named as x and y are given as inputs to OR entryway. Now, the output obtained at the OR entryway is given as input to AND entryway along with the third input which is named as z. The output obtained at the AND entryway is passed to a NOT entryway where the output is inverted and finally the output is O as shown in the Fig. 4.

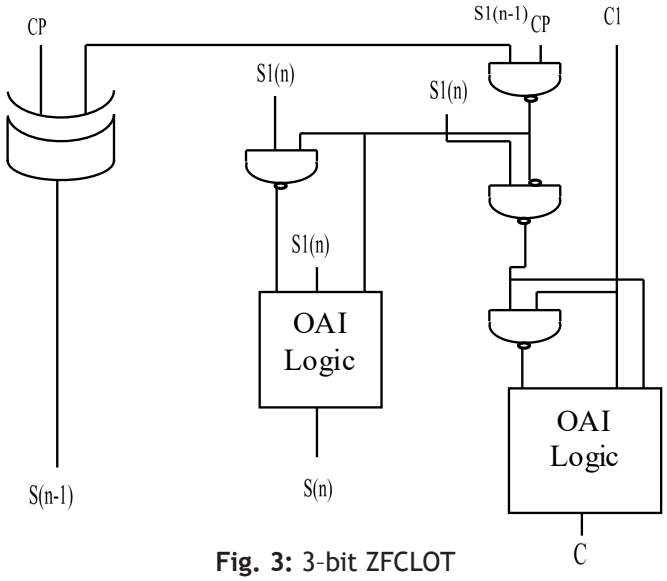


Fig. 3: 3-bit ZFCLOT

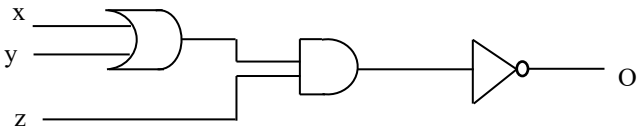


Fig. 4: OR AND INVERT (OAI) Logic

Results

The CSLA of 16 – bit utilizing ZFCLOT is carried out utilizing RCA of 2 – bit which has two full adders, a 2 – bit RCA 0, which has one-half adder and one full adder, a 3 – bit ZFCLOT circuit appeared in Fig. 3 and lastly 2:1 multiplexer. The activity of the circuits which are referenced above is recreated. The outcomes are noticed, checked and the outcome is as a waveform as demonstrated in the beneath pictures, and furthermore the circuit is being seen by RTL (Schematic Capture) as demonstrated in the below figures. There are two 16 – bit inputs, one carry input, one 16 – bit yield and a carry yield acquired at long last.

The 2 – bit RCA design is demonstrated in fig.5. It has two full adders named FA_0 and FA_n. 'A' and 'B' are the 2 – bit sources of info and Cin is the information carry, and Cout is the yield carry of 1 - bit, and 'sum' is the 2 – bit yield acquired after reproduction. The different blends for A, B and Cin are taken, and the yields Cout and total are as demonstrated in the fig. 6

The 2 – bit RCA 0 design is demonstrated in the fig. 7. RCA 0 is a circuit wherein the carry input is taken as '0'. It has one-half adder and one full adder named ha and fa. A and B are the 2 – bit contributions of a half adder, and ca, s are the comparing yields of half adder and these yields of half adder are given as contributions to the full adder. Presently, the full adder has inputs cin, x, y while the last yields got are c1, which is the carry yield and sum is the 2 – bit yield. The numerous mixes for A, B are taken and the yields 'c1' and sum are as demonstrated in the Fig. 8.

One of the principal blocks utilized in the CSLA utilizing ZFCLOT is 3 – bit "OAI Logic". In this rationale, the initial two sources of info are gone through an OR entryway, and afterward the yield got here, and the third information is being passed to AND entryway, lastly, the yield here is transformed. It has three contributions as x(1), x(2) and x(3), as demonstrated in the fig. 9. For different mixes of sources of info, the yields are plotted as a waveform, as demonstrated in the Fig. 10.

In ZFCLOT, A, B are taken as sources of info and cin is likewise taken as one of the information CP is the previous carry. ZFCLOT is carried out utilizing NAND entryways and OAI Logic (Or And Invert Logic). X, Y, and C are the resulting yields as shown in the fig. 11. The different blends of A, B, and cin are taken, and the outcome is a waveform as demonstrated in the Fig. 12.

The Schematic Capture of CSLA utilizing ZFCLOT is as demonstrated in Fig. 8. This is carried out and orchestrated utilizing 45 nm Cadence innovation instruments. Here, there is a carry information and two 16 – bit inputs. ZFCLOT is acquired by interfacing the RCA, RCA 0 and ZFCLOT segments with the assistance of a 2:1 multiplexer. At last, the outcomes acquired is a 16 – bit yield vector and a got carry. There are different components present in the Cadence technology. The below Table 3 shows the space occupied by each item in 45 nm Cadence platform.

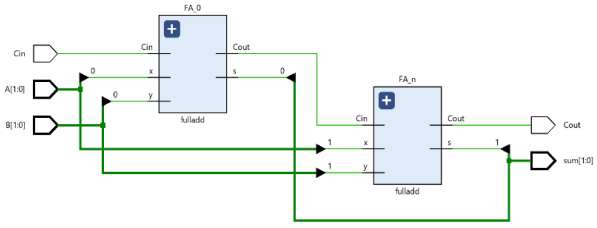


Fig. 5: Schematic capture of 2 – bit RCA

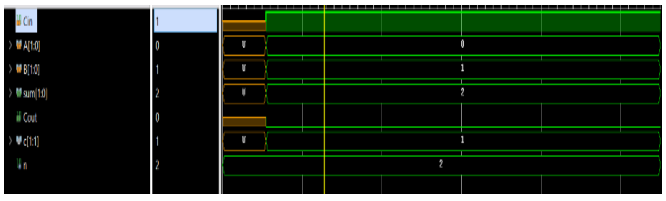


Fig. 6: Simulation result of 2 – bit RCA

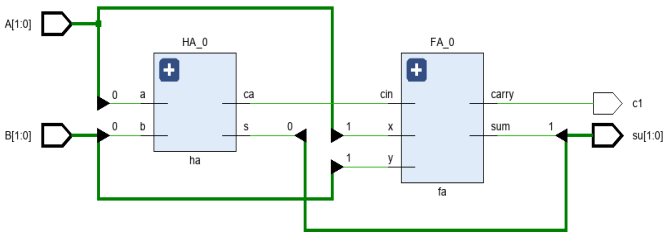


Fig. 7: Schematic Capture of 2 – bit RCA0

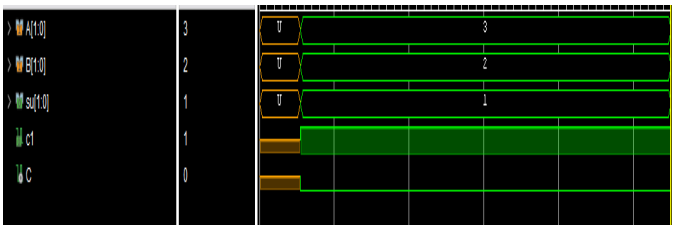


Fig. 8: Simulation result of 2 bit – RCA0

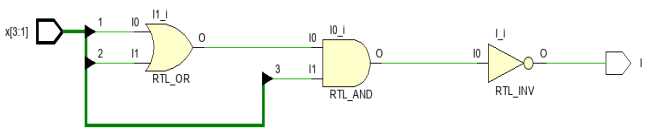


Fig. 9: Schematic Capture of OAI Logic

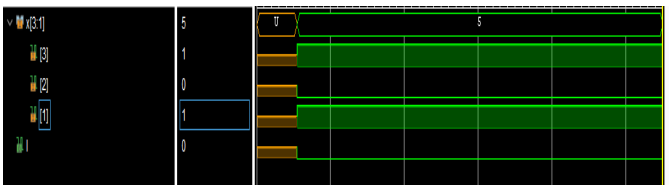


Fig. 10: Simulation waveform of OAI Logic

Module 0 has a ripple carry adder with two full adders and also another adder with one half adder and full adder. The below table 4 shows the space occupied by these two adders theoretically. The total space occupied by these two adders is about 384.7522 μm^2.

Dynamic and Leakage power are the main rule segments for complete power use. NAND entryway uses fewer semiconductors when appeared differently in relation to XOR & AND entrances. Thus, supreme power use is lessened. Application - Specific Integrated Circuit (ASIC) approach is utilized for acquiring the 3 – bit ZFCLOT. Various strategies are mulled over like Square Root CSLA, Square Root Binary to Excess CSLA converter, Square Root Zero Finding Logic CSLA, CSLALOT and ZFCLOT utilizing CSLA. These outcomes are recreated and are organized as demonstrated in the Table 4.

Fig. 13 shows the Dynamic Power comparison for various designs like Square Root CSLA, Square Root BEC CSLA, Square Root Zero Finding Logic CSLA, CSLALOT and ZFCLOT by CSLA. The designed Square Root CSLA (Sq Root CSLA), Square Root Binary to Excess Converter CSLA (Sq Root BEC CSLA) models by utilizing half adder and AND entryways. This half adder being planned by utilizing XOR entryways, AND entryways that involves high region and furthermore devours high power.

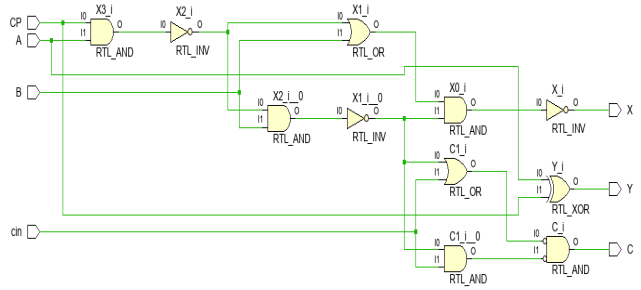


Fig. 11: Schematic Capture of a 3 – bit ZFCLOT

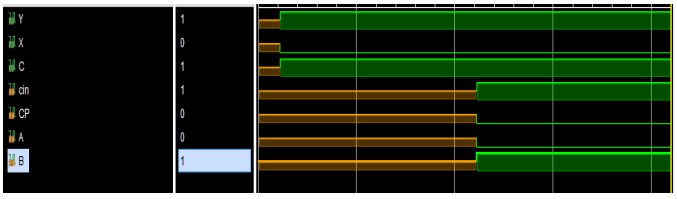


Fig. 12: Simulation waveform of a 3 – bit ZFCLOT

Full adder configuration assumes a vital part in the plan of all previously specified designs. According different investigations, it has been seen that different improvements have been acted in the perspective on full adder. In this manner, the full adder which consists of least region is given as an essential structure block in Cadence device library and utilized in plan of ZFCLOT by CSLA.

As examined before, a portion of the advanced parts are utilized in the plan of ZFCLOT by CSLA. Subsequently, Power Leakage, Dynamic Power and all out other powers are decreased. Fig. 14 shows the Leakage Power comparison for different designs like mentioned before. Fig. 15 shows the entire power correlation for various plans that is acquired by the addition of the spillage and the dynamic power. It is hard to lessen entire presentation measurements like space occupancy, power, and retardation. There should be compromise between space occupancy, power and retardation. Accordingly in the planned engineering, region and power improvements are done which expands defer which is the significant restriction for this design. Delay Products of Area and Power i.e. ADP and PDP are utilized to check the general exhibition of the engineering. ADP is acquired through increasing delay of area. Essentially, PDP is acquired through duplicating delay of power. Fig. 16 shows the Product Delay of Area (ADP). Fig. 17 shows the

TABLE 2: Key digital elements in 45 nm Cadence Technology

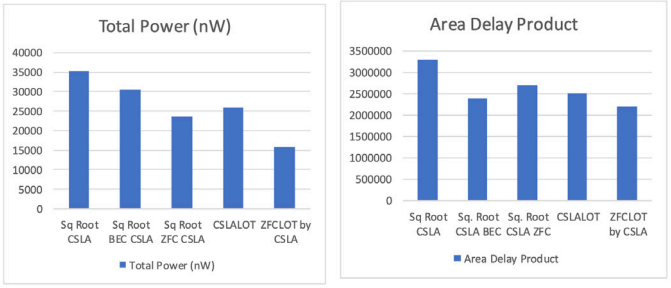
Digital Item	*Space occupied (μm2)*
AND Entryway	3.489
OR Entryway	3.489
XOR Entryway	6.258
2: 1 Mux	4.572
NAND Entryway	2.874
Half Adder	8.4736
OAI Logic	3.147
Full Adder	15.8756

TABLE 3: Theoretical Space Occupancy of CSLALOT

Ripple Carry Adder with two full adders	*Ripple Carry Adder with one half adder and one full adder*
It comes under Module 0	It comes under Module 1 to Module 7
The Space occupied is 26.8745	The Space occupied is 357.8777

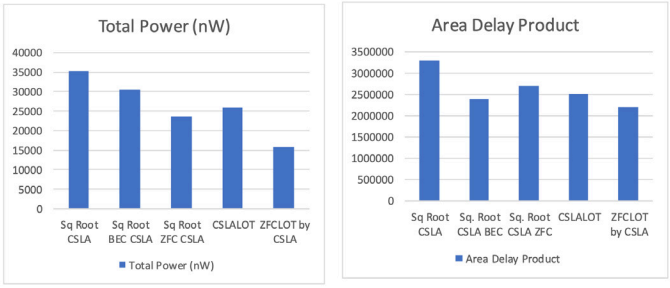
TABLE 4: ASIC outcomes utilizing Cadence 45 nm platform

Design	*Space Occupied (μm2)*	*Time Delay (ns)*	*Power Consumption (nW)*
Square Root CSLA	864.259	2968	35213.52
Sq. Root CSLA BEC	582.936	3654	30447.29
Sq. Root CSLA ZFC	568.412	5159	23593.605
CSLALOT	600.149	4527	25863.249
ZFCLOT by CSLA	410.268	5219	15874.204



(a) (b)

Fig. 13: Dynamic power comparison for various designs. Leakage Power comparison for various designs



(a) (b)

Fig. 14: **(a).Total Power Comparison for various** designs. (b). ADP Comparison for different designs

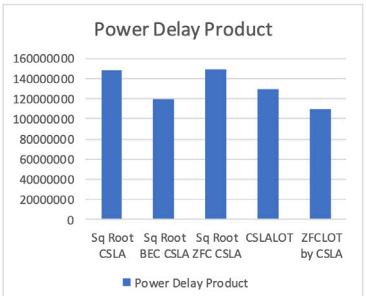


Fig. 15: PDP Comparison for different designs

Product Delay of Power (PDP). The above mentioned two delays, the CSLA utilizing ZFCLOT is low when contrasted with a condition to workmanship structures.

Conclusion

From this paper, we conclude that the VLSI construction is planned, recreated, and integrated utilizing Cadence platform for CSLA utilizing ZFCLOT. This design achieves the performance of area as 47.287% when contrasted with Sq Root CSLA. This design also achieves the performance of power as 49.1% when contrasted with Sq Root CSLA. This design also achieves the performance of area as 28.954% when contrasted with Sq Root BEC CSLA. This also achieves the performance of power as 36.2% when contrasted to Sq Root BEC CSLA. This design also achieves the performance of area as 16.424% and the performance of power as 14.459% when contrasted with Sq Root ZFC CSLA. This design also achieves the performance of area as 22.129% and the performance of power as 26.210% when contrasted with CSLALOT. Along these lines CSLA utilizing ZFCLOT is distinguished plan that is more suitable for less force, area productive processors of DSP. Subsequently in the planned design, region and power enhancements are done which builds delay which is the significant constraint for this design.

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