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FPGA Application: Realization of IIR filter based Architecture

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Abstract

This document investigation is performed on improved implementation of an Infinite Impulse Response (IIR) filter which can utilized practically. There are many other proposed models for IIR filters that yield promising and efficient results. The suggested IIR filter model known as a parallel-pipeline based on FIR filter. FIR filters on the other hand provide linear phase response, high stability, and limited precision errors. So, FIR based IIR filter offers better efficiency than its previous models. Moreover, there are other techniques such as the Two-Level Pipeline based IIR filter model and look-ahead-based model are mentioned and discussed. And the synthesis and results are obtained on a Xilinx Virtex-5 field-programmable Gate Array Board. After analyzing all design models mentioned, A new model for the implementation IIR filter is discussed which increases the efficiency of the filter.

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Introduction

Infinite impulse response (IIR) filters are everywhere utilized in digital signal processing systems for certain reasons. Analogue filters are comparable to IIR filters in certain aspects. IIR filters have complexity in computation similar times to FIR filters.[1-15] ASICs and signal processors architecture are tuned for filtering algorithms and put into effect for implementation of IIR filters. Applications of FPGAs are represented by IIR filters in the digital signal processing. Several advantages such as such as complete implementation in FPGA structure towards algorithm for filtering, higher output, effectiveness of hardware usage, precision by FPGA implementation of IIR filters. IIR filter solution for high-speed communication, image computing, and other special applications is FPGA. Properties of modern FPGAs for structure formation are mapping, optimization and depiction of data flow graphs.[16] In DSP, FIR filters have more importance. For construction of highly stable performance filters, unconditional stability and linear phase are useful characteristics. Sampling rate should be minimum two times the highest signal bandwidth according to Nyquist sampling rate. Speed is increasing more than 1GHz as, receiver high speed satellite broadband and increase in data transmission rate in communication system of high speed wideband. FIR filter implementation standards are raised. For many high-performance applications FPGA's internal logic has become first option because of flexibility in structure and reconfigurability and in addition to that development in technology and science also helping this out.[17-20] 740MHz is the max speed limit of computation of Xilinx Virtex-7. Filter's implementation structure is improved to attain more than 1GHz sample rate by usage of serial methods. For implementation in FPGAs requirement in speed can be reduced by usage of parallel processing. Discussion of structure of parallel filters is more in recent times. FIR filter fixed coefficient optimization technique is discussed. To improve speed of operation of filter, complexity of computation of FIR filter is reduced and decomposition of filter coefficient to a power of 2 carried out in this method. Convolution of linearity in matrix form utilized is used in Number of multiplications performed, cost of hardware can be reduced by placing delay elements regularly and usage of algorithm of fast linear convolution. For reduction of filter resources based sub-filters of two-stage method

is proposed. This requires adders and delay elements in large numbers.[21-29]

Proposed Models

Look Ahead Pipelining IIR filter Implementation

Implementation of the Digital Infinite Impulse Response Filter using look-Ahead technology is highly utilized in high-speed systems [19]. The thought of Look-Ahead technology is for to sum up or delete poles and 0's towards Transfer function so the denominator coefficients belonging to Transfer function become zero. Therefore, it increases the clock speed. Staged loops increase complexity of the system. Fig.1 shows filter implementation [30]-[35].

Taking into account, the Transfer Function of the first Order digital IIR filter as:

$$H(Z)=\frac{1}{Z}*\frac{Z}{(1-a)} \quad (1)$$

|a| ≤1, for condition to be stable. It has place 1 pole at z=a. Then, differential equation is as follows

$$y(n+1+0)=x(n)+y(n) \quad (2)$$

Then,

$$y(n+2+0)=y(n+0+1)+x(n+1+0)$$
$$=a2y(n)+x(n)+x(n+0+1) \quad (3)$$

Two-Level Parallel Pipeline IIR Filter

Limitation of pipeline process is communication and sample speed cannot be increased at terminal point. If these limitations are overcoming pipelining process could be utilized to improve critical path computation. Sample speed can be increased by mixing pipelining and parallel processing. The sample speed is increased a lot as lot of outputs are obtained at one clock speed in parallel processing technique. If one method used is pipelined technique for a calculation then other used technique is parallel to obtain calculation. For various methods computation these two methods are present. One set at a time is calculated in pipelining method in between the line's mode in Resemblance hardware process calculation s is done in parallel processing. As a result, by cross product of L and M high sample rate is obtained for Parallel pipeline IIR filter, where L is processing levels of block and M is stages of pipelining. Representation of Ten sample speed is

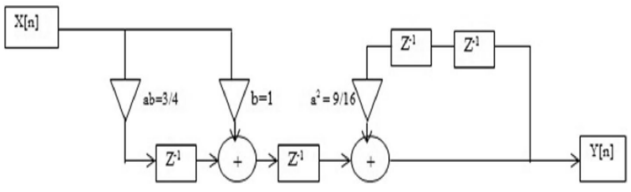

Fig. 1: Look ahead pipelining IIR-filter.

$$T_{sample}=T_{clk}/M \quad (4)$$

2-parallel (L=2) and 2-pipeline (M=2) (L=2) levels are realized by review of the design. The required operation is one loop update as filter order given is one. Delay element is represented as block level and sample period of two times is the clock period of this block level in parallel processing. As a result, output y(n) and input x(n) sequence should be improved as y(n+2) is changed. Odd and even sequences are a result of dividing Eq. (4). Let, odd sequence is n=2 k–1 and even sequence is n=2 k.

Depiction of even equation is

$$y(n+0+2)=y(2k+0+2)=$$
$$=x(2k)+x(2k+1)+a(6)\cdot 2y(2k) \quad (5)$$

Depiction of odd equation is

$$y(n+0+2)=y(2k+0+1)=$$
$$=x(2k-1)+x(2k)+a(7)\cdot 2y(2k-1) \quad (6)$$

Execution of parallel pipeline IIR filter is based on equations (6) and (7). In Fig. 2 Two-level parallel-pipeline IIR planning is depicted using the above equations. ¾ is the coefficient 2 non recursive parts, 9/16 coefficient is for 2-recursive parts with two-unit delays, ¾coefficent for two non-recursive parts.

Z=a is location of pole in the original system while, z=a2 is the location of pole in parallel. As |a2 |≤|a| (since |a|≤1), it is closer to origin. To the round of noise strength of the architecture evolved at this movement of pole.

Proposed FIR based IIR Filter

Because of innate properties within the IIR filter architecture, the systems face limitations. By the usage

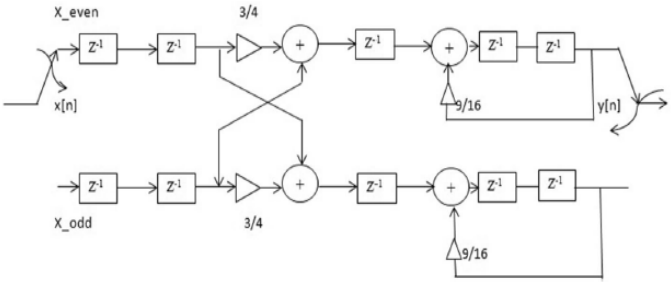

Fig. 2: Parallel-pipelined two-level implementation of IIR filter.

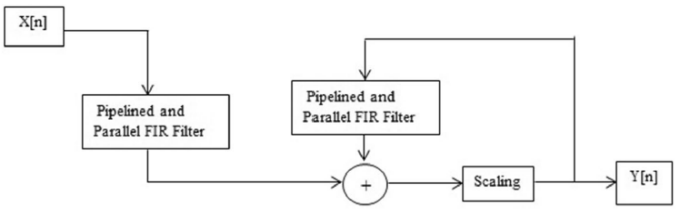

Fig. 3: Block Diagram.

of parallel-pipeline FIR Filters including scaling factor, high output IIR filter can be obtained. By combining 8 tap parallel pipeline FIR filters can be converted to high speed IIR Filter structure. Performance can be improved by this process. Fig.3 shows the depicted method [36]-[43].

Two addition and one multiplication operations are used to calculate least time needed for critical delay. The time utilized for multiplication and addition operations, respectively is TM and TA then (T-sample) is

$$y(n) = a\ (n+0) + b\ (n-1+0) + c\ (0+n-2) \quad (7)$$

$$T_{sample} \geq TM + 2TA \quad (8)$$

or sample frequency is

$$f_{sample} \leq 1/\ TM + 2TA \quad (9)$$

To all multipliers the data are transmitted in above mentioned formation. By this critical path can be reduced a lot. TM +TA is the formula to calculate critical delay of path. Sample frequency is increased by this method. Fig. 5 depicts the mentioned filter. Fig. 6 shows the combination of date-transmit, fine-grain and parallel pipeline processing. To decrease the critical path, parallel inputs of 3(quantity) are there in FIR filter and usage of 2-pipeline delay for reduction of critical path. For further reduction in critical path fine grain pipelining in parallel filter is used. To attain the high clock speed, the multiplier unit is separated into two small units (m1, m2) and also a latch is fixed in between the two units in fine grain process. This results in sample period reduction by.[22]

$$T_{sample}\ 1/6(TM + TA) \quad (10)$$

For lower power consumption parallel processing and pipelining techniques are used. In one clock cycle

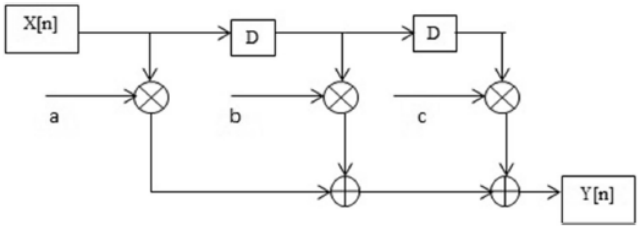

Fig. 4: Diagrammatic depiction of FIR filter of 3 tap.

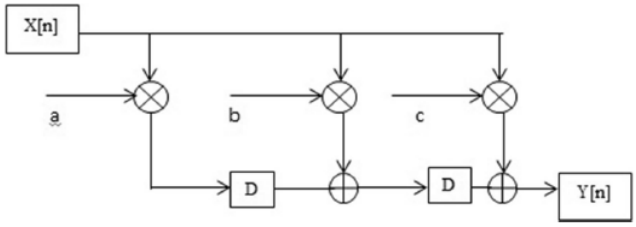

Fig. 5: FIR filter (3 tap) structure of data broadcast

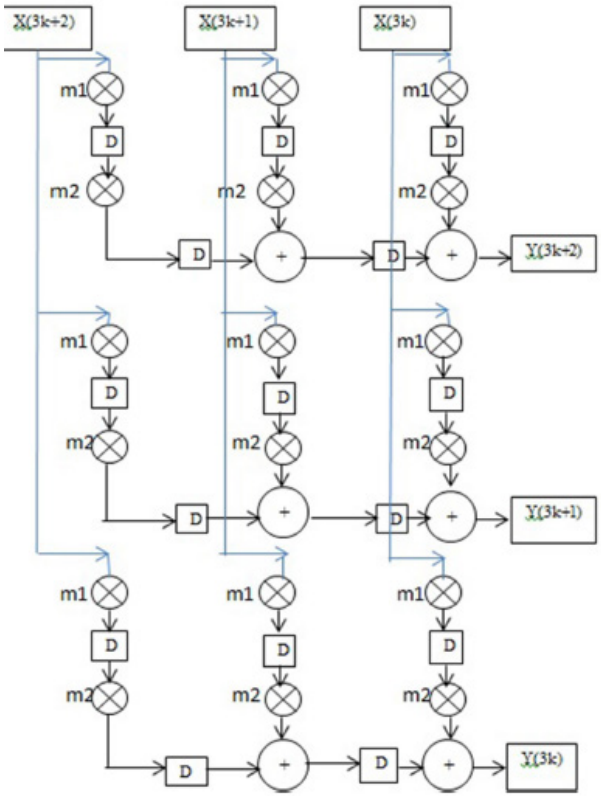

Fig. 6: Proposed FIR based IIR filter.

Table 1: Analysis by proposed models

Parameters of synthesis	*Look ahead IIR-filter*	*Parallel IIR-filter*	*Proposed FIR basis IIR-filter*
Quantity of Slice-Registers	180	192	172
LUT quantity	145	135	120
IOBs quantity	31	45	35
BRAMS	8	10	8
DSP8Es	18	20	16
Power (W)	0.150	0.180	0.120
Speed (MHz)	172.280	245.306	285.105

capacitance is discharged or charged results in reduction by usage of pipeline technique whereas Clock cycle is increased for discharging or charging capacitance in parallel technique. Power consumption decreased because of clock lines as compare High speed clock is used in pipeline system for the sample speed.

Simulation Results And Experimental Findings

As it is mentioned earlier, there are multiple ways in the implementation of digital Infinite Impulse Response filter but the purpose of the implementation is to provide much more efficient filter.[6] The implementation is based on FPGA design technology, analysis of proposed models is shown in tabular column.

Implementation and Design

For a limited period of time, impulse response h(t) does not equal to zero after a specific point. This is differentiated as IIR is considered a property of digital filters to many Linear Time-Invariant systems. As an example, if there is composition of inductors, capacitors, resistors in an electronic filter of analogous nature then it can be considered as an IIR filter. Filters which are digital having tapped delay lines with no feedback can be called FIR filters.

Transfer Function Derivation

$$y(n)=\frac{1}{a_n}\left(\begin{matrix}b_0x(n)+b_1x(n-1)+\cdots+b_px(n-p)-\\ a_1y(n-1)-a_2y(n-2)\cdots-a_0y(n-q)\end{matrix}\right) \quad (11)$$

The resulted transfer function is defined as:

$$H(Z)=\frac{Y(z)}{X(z)}=\frac{\sum_{i=0}^{p}b_iz^{-i}}{\sum_{j=0}^{q}a_jz^{-j}} \quad (12)$$

Stability

Transfer function can be used to check if the system is BIBO stable or not. Unit circle should be included in ROC to acquire BIBO stability.

Example: All poles have to be smaller than unity in a casual system.

$$H(Z)=\frac{\sum_{i=0}^{p}b_iz^{-i}}{1+\sum_{j=0}^{q}a_jz^{-j}} \quad (12)$$

Results

After implementing the circuit shown in fig.7,with input x and variable clock and reset pins. We can observe output at y shown in Fig. 8 and Fig. 9

Fig. 1.

Conclusion

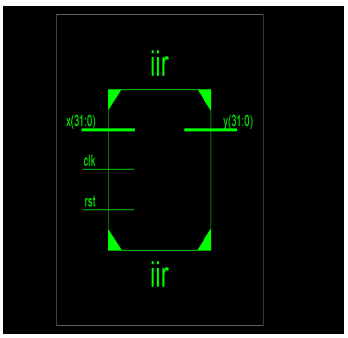

Fig. 7: Block Diagram of IIR filter

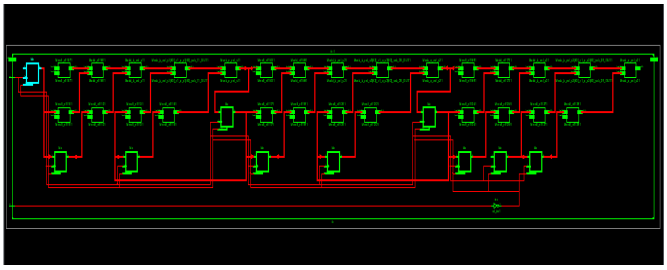

Fig. 8: Circuit diagram of IIR filter

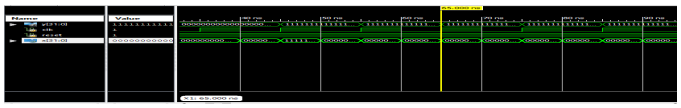

Fig. 9: **Output with clk=0 and reset=1.**

Fig. 10: **Output with clk=1 and reset=1.**

This paper investigates the improved implementation of an IIR filter which can be utilized for practical usage. There are many other proposed models for IIR filters that yield promising and efficient results. The parallel-pipeline suggested finite impulse (FIR) filter is also known as IIR filter design. FIR filters on the other hand provide linear phase response, high stability, and limited precision errors. So, FIR based IIR filter offers better efficiency than its previous models. Two-level pipeline-based IIR filter model and look-ahead-based model are mentioned and discussed are two other techniques.

This paper investigates the improved implementation of an IIR filter which can be utilized for practical usage. There are many other proposed models for IIR filters that yield promising and efficient results. The parallel-pipeline suggested finite impulse (FIR) filter is also known as IIR filter design. FIR filters on the other hand provide linear phase response, high stability, and limited precision errors. So, FIR based IIR filter offers better efficiency than its previous models. Two-level pipeline-based IIR filter model

and look-ahead-based model are mentioned and discussed are two other techniques.

Xilinx Virtex-5 field-Programmable Gate Array Board is used for synthesis and results. After analyzing all the design models mentioned, A new model for the implementation IIR filter is discussed which increases the efficiency of the filter.

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