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Research Article

HIGH SPEED AND RELIABLE DOUBLE EDGE TRIGGERED D- FLIP-FLOP FOR MEMORY APPLICATIONS

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ABSTRACT
In this paper we designed a low power and high speed phase detector using the positive edge triggered D flip flop. the proposed architecture consists of the 16 number of transistors and it consumes the very less power 10.25uw with the phase noise -150.45db respectively with offset frequency of 1Mhz. The circuit also tested the different corners in order to analyse the reliability of the circuit(TT,FF,SS.SF,FS) respectively.

Keywords: Phase detector, D-Flip-Flop, Phase noise.

INTRODUCTION

As the day by day technology has been scaling down towards micrometers to nanometres then behaviour of the circuit performance has greatly effects on electronic circuit behaviour. power consumption and high speed are two major parameters in present day electronic world and greatly impact on performance of the circuit[1-3]. A great research has been going on over the past decade to improve the performance of the electronic devices by reducing the complexity of chip area and power consumption. Flip-flops are the a set of sequential circuits, which has a great attention in present day scenario. D-flop flop is one of most important building blockand places a major role in digital circuits especially in VLSI. Different D-Flip-flops have been proposed by the multiple authors to increase the speed and to reduce the power consumption.the estimation of the power dissipation in the DFF is expressed by below expressions 1.

$$P_{avg}=P_{Short\text{-}circuit}+P_{switching}+P_{lekage} \quad (1)$$

The structure of D-flip flop has been broadly divided in to two categories such as static and dynamic respectively. Over the years it has paid a lot of attention towards the a bulk of applications such as Flip- flops are widely used in several applications such as memory blocks, phase detectors, cryptography ,analog to digital converters etc. In this paper we are mainly focused on design of phase detector using the D-flip flop to accurately estimate and detect the error signal[4-6].The paper is organised as follows:Section2 to describes the basic operation of the phase detector and different types of D- flip flops and section 3 describes the operation of the proposed D flip-Flop .Section 4 describes the simulation results, corresponding layout and final section describes the conclusion of this paper.

Conventional Phase Detector

Figure 1 depicts the block diagram of the conventional phase detector using the D flip flops. It consists of two D flip flops and one and gate respectively. Fref and Fvco will acts as a clock signal for the top and bottom D flip flops. A n input VDD will given to the two DFF at same time period and whose final output is going to given to the input for the and gate in terms of UP and DOWN. in order synchronise the clock frequency and to enhance the parameters of the phase detector a different set of D flip flops being used. the role of the AND gate is very less and it has impact less significance on performance of the phase detector[7].

Analysis of Different types of D-Flip- Flops

In this section we are going to explain the different types latches and flip flops which can be used for the optimization of the power consumption and area. For any type of the D flip flop its speed can be limited by their transconductance. In order to detect the error and their performance has greatly effect on the type of the D flip flop respectively.

SET D Flip-Flop

Conventional D SET Flip-Flop operates on both edges (rising edge and falling edge) of the clock. To operate the D-Flip-Flop it has maintained before the setup time and after the hold time of the rising edge of the clock. the structure of the 16 transistors and a PMOS transistor can be used to be feedback in order to reduce the noise. This structure dissipate the huge amount of power and occupies the more area on the chip respectively[8].

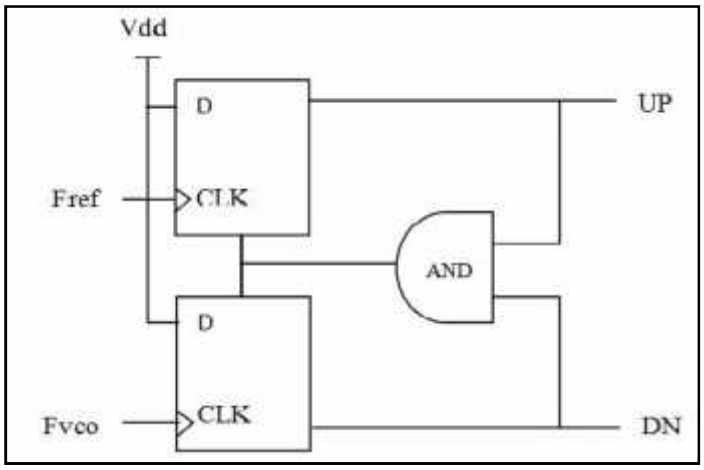

Figure1: Circuit diagram of Phase Detector

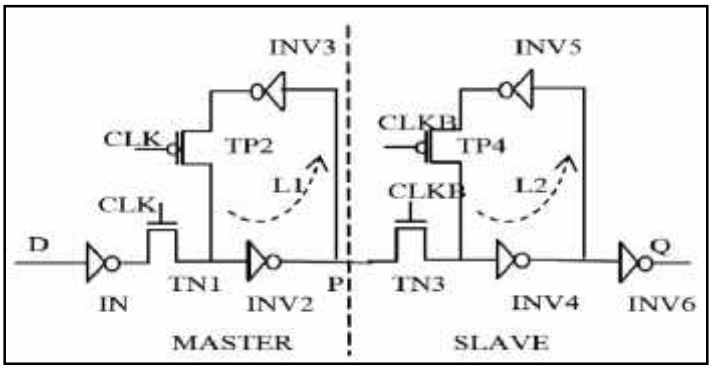

Figure 2: SETD FLIP-FLOP.

2.10 transistor SET D Flip-Flop

The design consists of 10 transistors with negative edge triggered SET D Flip-Flop[]. Here we eliminated the slave section and connected a transmission gate at feedback. During the operation the final data and intermediate data is stored in node X. When the clock is active LOW the Latch is on primarily on static nature and it has proven that 10 transistor D flip flop on continuously on state. The structure of the SET D flip flop as shown in figure 3 respectively[9].

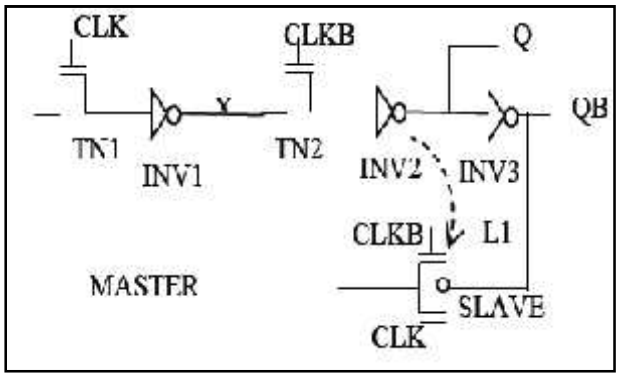

Figure 3: 10 TRANSISTOR SET D FLIP-FLOP.

4.TSPC (True Single Phase Clocked) D-Flip-Flop:

The TSPC D- flip flop as shown in figure 4, it consists of total nine transistors ,the clocked transistors are kept nearer to the power supply and ground. The state transition usually occurs at the rising edge of the clock signal.whenever the D=0 and Clk=0 the output becomes 1(Qb). as a result MPS1,MPS2 and MP1 are turned on. And whenever the clock changes from low to high and D=1 Qb becomes low[10].

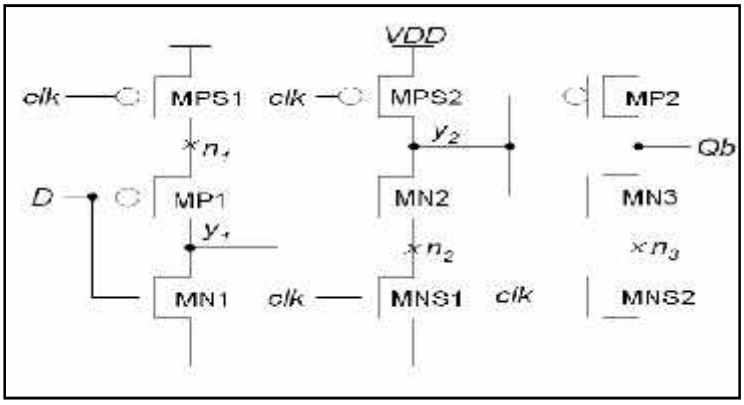

Figure 4: TSPC D Flip-Flop.

Proposed positive edge triggered D Flip-Flop

Here we proposed positive edge triggered D flip-Flop whose configuration is elaborated in two stages. Such as the master and slave stages using the D latches. The master stage composite of eight transistors in which two tristate inverters are replaced by the two transmission gates along with inverter connection. Its operation is similar to the D Latch. when the clock is active high input follows the master state and when the clock is changes from high to low it changes its state from high to low and it follows the slave state. Figure 5 depicts the circuit diagram of the proposed D flip-flop.

Results and Discussion

Below figure represents the transient power analysis of the proposed D flip-flop has 10.36uw and which is very less as compared to the conventional architecture and it can be operated low electronic devices where it consumes the less power and very high speed applications. and also estimated the output frequency at 1 MHz calculated the its phase noise and was represented in figure 8 respectively.

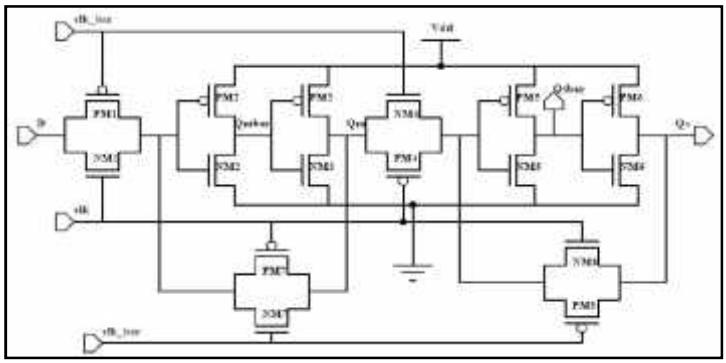

Figure 5: Proposed positive Edge triggered D Flip-Flop.

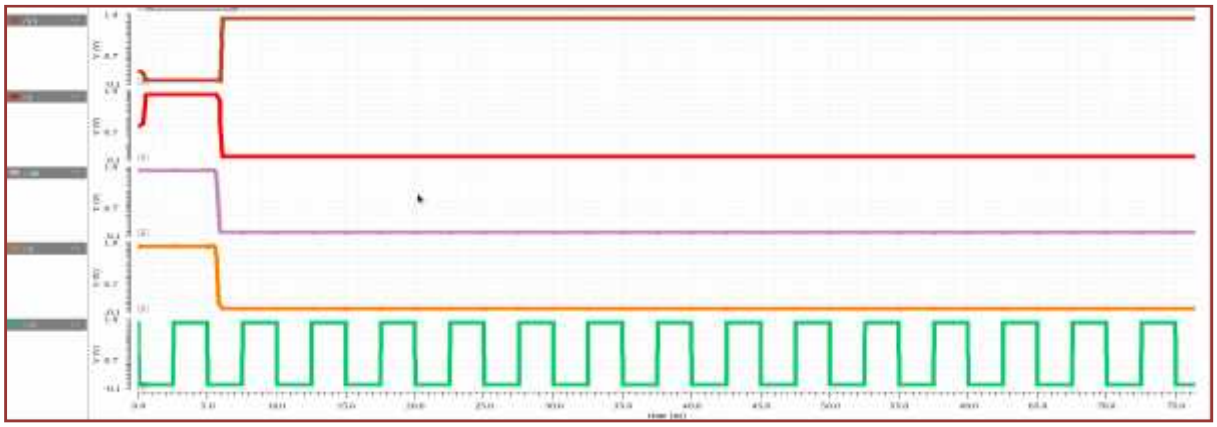

Figure 6: Proposed D flip-Flop transient analysis

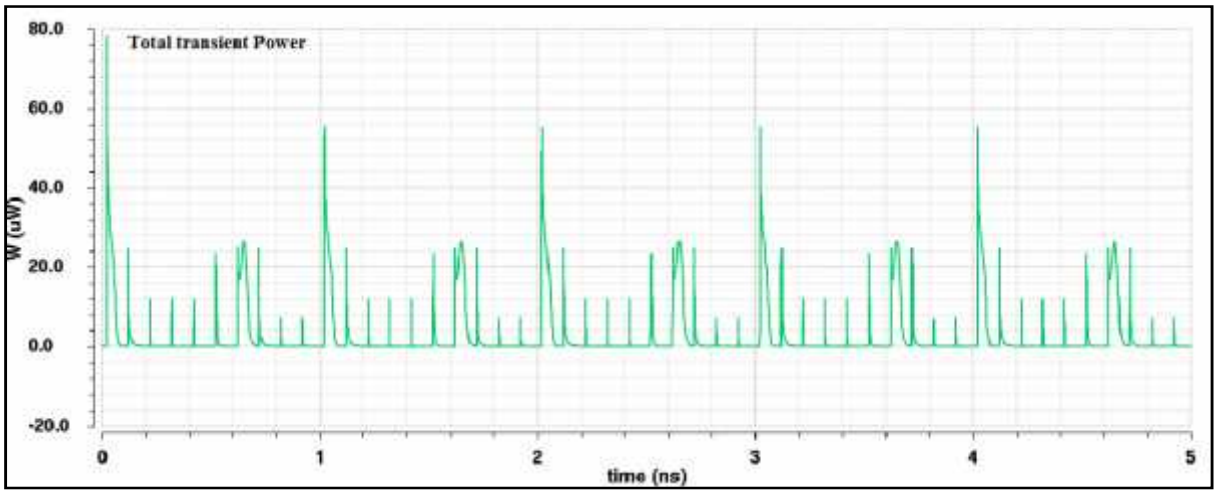

Figure 7: Proposed D flip-Flop power analysis.

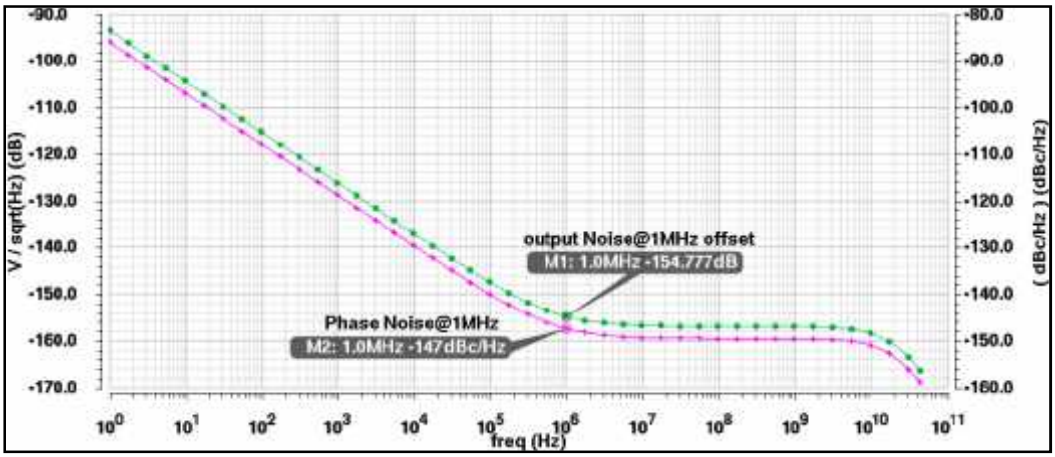

Figure 8: Proposed D flip-Flop phase noise analysis.

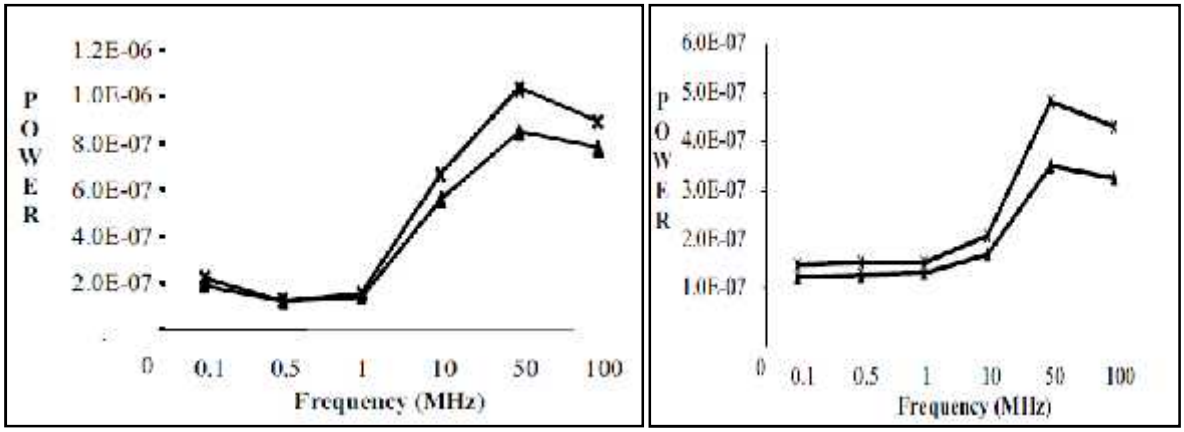

Figure 9: Proposed D flip-Flop power analysis.

Conclusion

The proposed positive edge triggered SET D flip-Flop is designed and tested using the 180nm technology and simulated using the cadence spectre simulator. The circuit can be simulated at very high frequency(5GH to 10Ghz) and it satisfies the required conditions. It can be highly suitable for the phase detectors, clock and data recovery applications etc.

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