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XOR Module based Adder Applications Design using QCA

Lau W. Cheng[1], Beh L. Wei[2]

[1,2]Faculty of Information Science and Technology University, Kebangsaan, Malaysia

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Abstract

Quantum-dot Cellular Automata (QCA) is a piece of optimistic machinery that provides an advanced design for resolving all arithmetic schemes at appreciable nanotechnology. In this paper, based on cell interaction, a novel based three-input XOR gate is designed. For general-purpose task by fixing one of its inputs to two-input XOR gates to achieve. With the help of a 3-input XOR gate, a compact full adder is designed. Besides, we concentrated on creating a Novel for an 8-bit controllable inverter using QCA. All functionalism and performance of the methods can be visualized using the QCA Designer tool. In addition to this, diversified power dissipation characteristics are observed from the QCA Designer tool simulator.

Author's e-mail: Lau.wai@ftsm.ukm.my, beh.lee@ftsm.ukm.my

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Introduction

CMOS applications are being developed with the promising alternative of QCA technology. This QCA is the CMOS technologies at the nanoscale for designing digital circuits. QCA has more benefits than CMOS, and it is executed with the semiconductor of the QCA.[1-13] QCA represents the polarization of electrons and has better advantages over CMOS technologies. We are implementing our Novel controller in the Quantum-dot Cellular Automata (QCA) for high performance nanotechnology. Design and implementation are done in the QCA designer tool.QCA is more attractive for its size, speed, feature, highly scalable, low power consumption than CMOS technology. It represents a binary state of '*0*' and '*1*', which generate inputs and output the QCA cell. In this study, we resolve the components and logic gates recycled for QCA circuits. The executed 2-input "XOR" circuit took up a small field with a lower complexity of 10 cells. All the designs are implemented in the QCA tool.[14-27]

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} \quad (1)$$

Where P is Polarization and P_i means electron charge.

QCA is a nuclear, square structure that includes 4 quantum dots & 2 surplus electrons assembled from semi-conductive substance.[8] In the cell, two stable states are formed, as shown in Fig. 1(a). The two stable states are polarization (*-1*) means *logic 0*, polarization (*+1*) means *logic 1*. For calculating the polarization, we use the formula

The transmission of information in QCA is done with the help of neighboring cell interaction which is called as QCA wire. These Cells are rotated (45°) degrees, as depicted in Figs. 1(a), (b). Execution of upturned chain and wire-crossing basis in QCA [9]-[11], Fig. 1(c) and Fig. 1(d). QCA clock signals are consummate by synchronization and timing. The channel of sequential and combinational circuits requires adiabatic four-phase clocking signals. The Clock signals control the entire QCA wires and provide

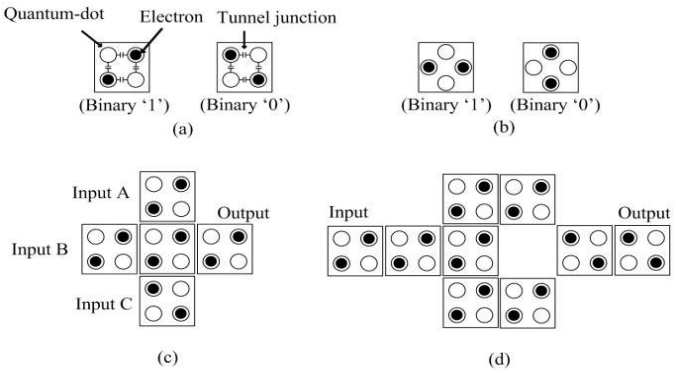

Fig. 1: QCA key cells: (a) Formal (b) twisted (c) majority gate, (d) powerful inverter, (e) clocking of QCA

power to the channel layout.[12-14] We Can do wire crossing by using two quantum dot directions, and they allow wire perpendicular to other types of wire. These two types of cells have them function on propagates polarization without change, other reverse polarization from an adjacent cell to next. However, the length between item is uniform. The crossbar technique is a new implementation of QCA, which gives a unique perspective on QCA clocking.[28-31]

Existing Model Analyses

We have an existing *XOR* gate, a full adder, a controllable inverter, and ripple-carry adders using CMOS technology. We can design CMOS structures, but we have certain complexities that face while implementing item: *XOR* gates provides slow switching speed. We can structure full adder in different forms and would to various disadvantages while designing the circuits.[32-43]

Full adder has disadvantages include large power consumption, a large chip area and high input data, i.e. large transistor count. Ripple carry adder disadvantages include wiring complexity, high delay and into suitable for low power applications. The most significant drawbacks of these ripple-carry adders are increasing delay time linearly with the bit length. The controllable inverter has the speed limitations of CMOS technology.[44]

The Proposed Structures

Designed XOR gate

XOR gate can be abbreviated as the exclusive-OR gate. XOR gate is a digital logic gate that functions depends on inputs provided to it. It gives output as '*1*' when inputs given are odd. The circuit design and output expressions of the 2-input XOR gates and 3-input XOR gates are described as follows:

$$A \oplus B = AB' + A'B \tag{2}$$

$$A \oplus B \oplus X = ABC + A'B'C + A'BC' + AB'C' \tag{3}$$

Designed Full Ladder

A full adder performs addition and is realized with illogic gates. A full adder has three one-bit binary numbers, two operands and a carry bit. Using full adder circuits, we get total swing output; the power consumption is less. Mainly these are robustness to supply voltage scaling and also have high speed.

$$C_{out} = Maj(A, B, C_{in}) \tag{4}$$

$$Sum = Maj(Maj(A, B, C_{in}), Maj(A, B, C_{in}), Maj(A, B, C_{in})) \tag{5}$$

Designed ripple carry adder

Ripple carry act as an inefficient mechanism for large numbers; it is easy to carry out with small several bus and design. The diagram of the Ripple carry adder is straight forward also have fewer connections. The sequential circuit is designed in items of area, delay, power and testability.

For standard transmission, the circuit consists of 1093 cells. As the multiplication delay of the design develops, the field turns more prominent. The field covered through the executed RCA is 1.8μm^2.

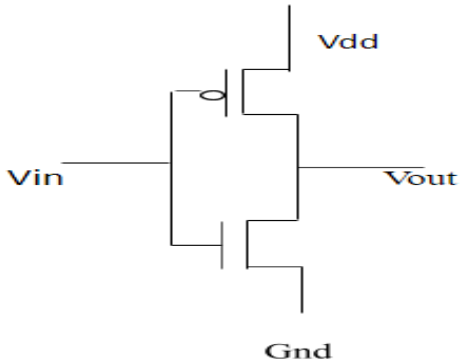

Fig. 2: Inverter using CMOS technology

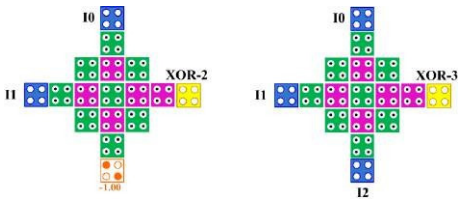

Fig. 3: XOR gate layouts: (a) 2-input XOR, (b) 3-input XOR

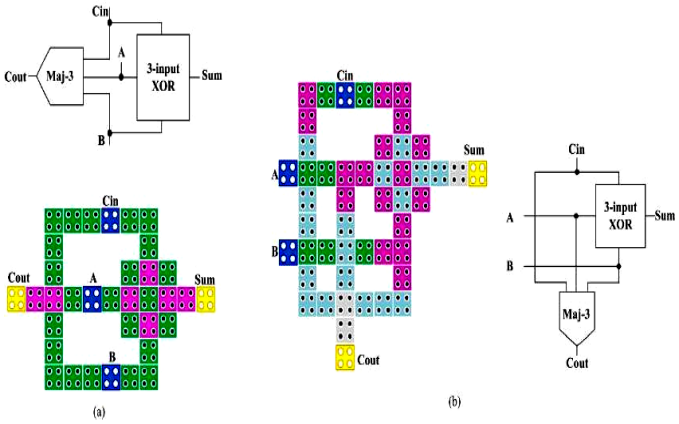

Fig. 4: Expected full adder: (a) simple layout, (b) extensible layout

Table 1: Truth table of the XOR gate

A	*B*	*XOR (A, B)*
1	1	0
1	0	1
0	1	1
0	0	0

Designed Eight-bit controllable inverter

The controllable inverter is also called a controlled buffer and NOT gate. It is used in-between bus and output, so line control checks the result is fed to the bus or input. We can implement the controllable inverter by using universal gates. The inverter is designed neither using an X-NOR gate when either its one input is low. Finally, these three gates are used as an inverter. The controllable inverter is also called both a controlled buffer and a NOT gate.

Simulation Results

Output Waveforms of XOR Gates

The output of XOR gate 2-input results the first 2 waveforms represent the input sources as I_1 and I_0 and third waveform represent the output of XOR-2 gate and remaining waveforms represents the different clock signals as shown in Fig. 9. Similarly in the output of XOR gate 3-input results the first 3 waveforms represent the input sources as I_1, I_2 and I_0 and third waveform represent the output of XOR-3 gate as shown in Fig. 10.

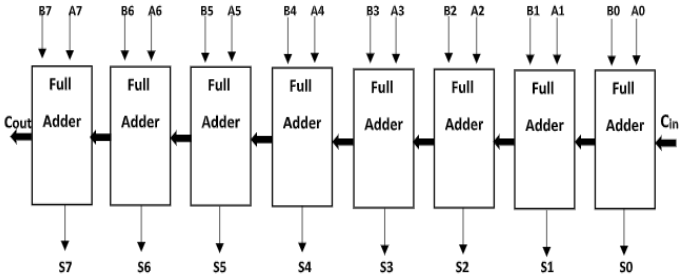

Fig. 5: Schematic layout of Eight-bit Ripple carry adder layout

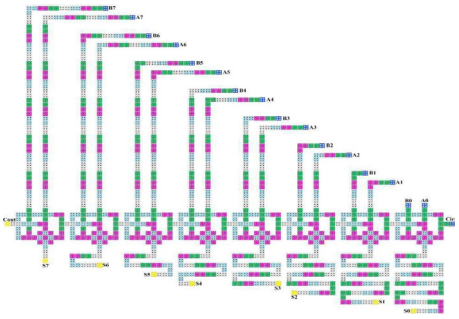

Fig. 6: Eight-bit Ripple carry adder (RCA) design

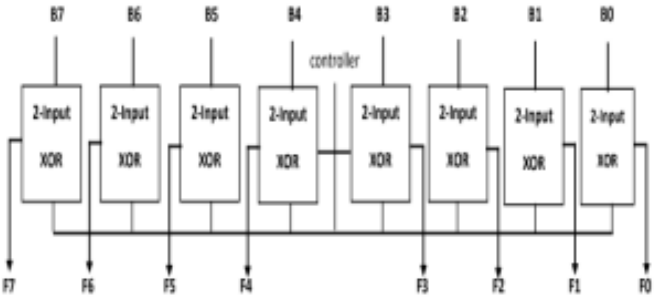

Fig. 7: Schematic drawing of an Eight-bit controllable inverter

Output waveforms of Full adder (Fig. 9 & 10)

Output waveforms of ripple carry adder (Fig. 11)

Output waveforms of controllable inverter (Fig. 12)

Power Dissipation Analyses

It is observed the reliable performance and other characteristics of the proposed designs using the QCA designer tool version. 2.0.3. A 3-input XOR gate is examined for illustration, as depicted in Fig. 9 proceeds with three

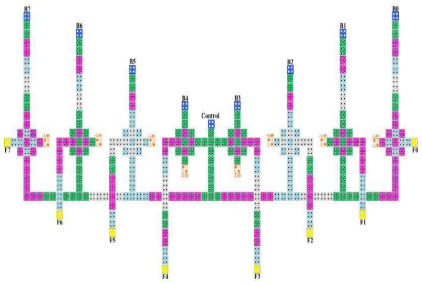

Fig. 8: Designed Eight-bit controllable inverter scheme working ion QCA

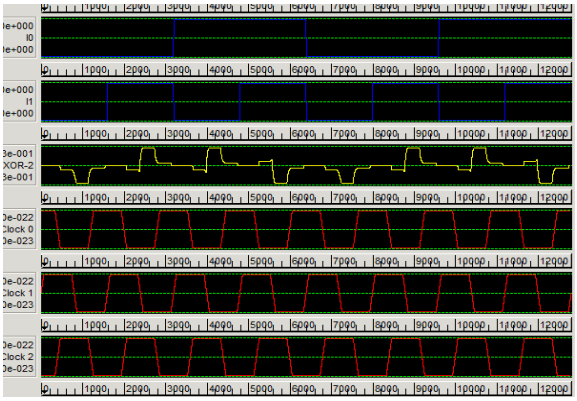

Fig. 9: Simulation outcomes of the designed XOR 2-input gate

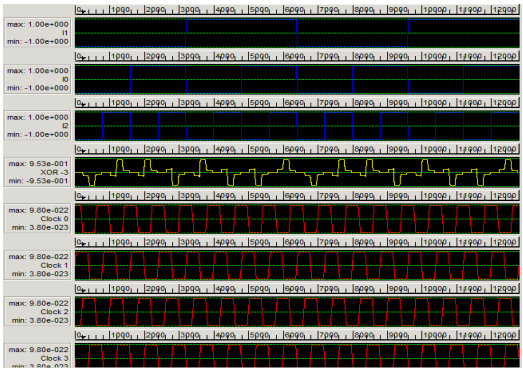

Fig. 10: Simulation outcomes of the designed XOR3-input XOR gate

data inputs A, B, and C to setup output *XOR_3 = ABC + A'B'C + A'BC' + AB'C'*. Power dissipation of XOR layout is measured using QCA layout, input/output vector set, and switching vector set.

The simulation results shown in Fig. 13 for the inverter has in good agreement with the optimized, reliable results of delay reduction and the output is made available almost at 1.74 clock cycles. The same compact layout is being developed with the XOR based cell interaction method. In table 2, multilayer is represented as M and coplanar is represented as C.

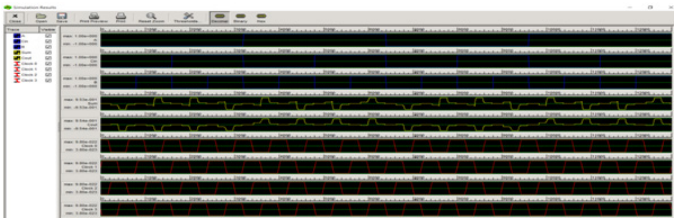

Fig. 11: Simulation outcomes of designed full adder.

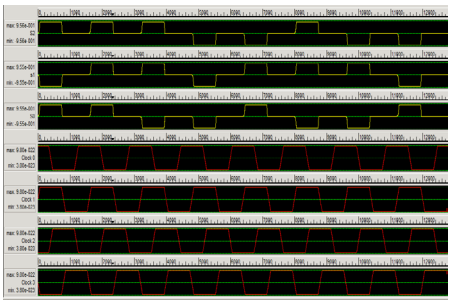

Fig. 12: Simulation outcomes of the RCA

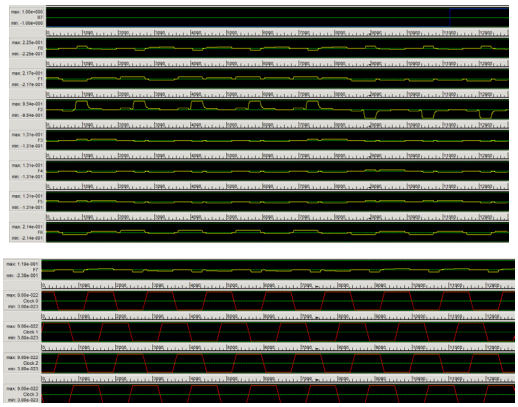

Fig. 13: 8-bit inverter simulation results.

Table 2: Identification of bi-stable comparison

Specifications	*Values*
Maximum iteration per sample	110
Cell size	18nm
Radius of effect	65nm
Dot diameter	5nm
Number of samples	50K
Clock ow	3.8e-23J
Relative permittivity	12.9
Clock igh	9.8e-22J
Layer separation	11.5nm

Power dissipation and polarization of the QCA cell operates on quantum mechanism estimated by a Hamiltonian matrix. The Hamiltonian matrix uses Hartree-Fock similarity to determine power study for a collection of similar data of QCA cells as follows:

$$H_i = \begin{bmatrix} -E_{K^2}\sum_i C_i f_i & -\gamma \\ -\gamma & E_{K^2}\sum_i C_i f_i \end{bmatrix} = \begin{bmatrix} -E_{K^2}\left(C_{j-1}+C_{j+1}\right) & -\gamma \\ -\gamma & E_{K^2}E_{K^2}\left(C_{j-1}+C_{j+1}\right) \end{bmatrix} \quad (5)$$

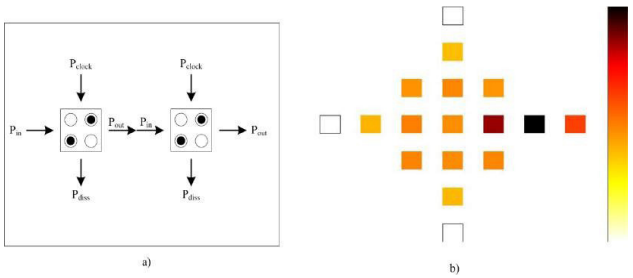

Fig. 14: Displays (a) energy flow,(b) the power dissipation design of the three-input XOR gate

Table 3: Observation outcomes of the 3-input XOR gates

Cell	*Count*	*Total area (μm²)*	*Delay*
XOR-3[3]	69	0.082	7
XOR-3[4]	97	0.092	4
XOR-3[5]	26	0.19	2
Proposed	17	0.014	1

Table 4. Similar Results of the full adder

Design	*Cell*	*Count*	*Delay*	*Cross overtype*
[1]	73	0.039	4	M
[2]	52	0.029	4	M
[3]	37	0.019	4	M
[4]	30	0.019	4	M
[5]	60	0.029	4	C
[6]	39	0.029	3	C
Proposed	35	0.02	3	C

Conclusion and Futurescope

XOR gate with three inputs are considered in this article to develop the cell interaction method. The essential objective in this project is to propose a modern, and high-speed i8-bit controllable inverter and Ripple carry adder (RCA) designs accordingly. The incomplete hierarchical i8-bit controllable inverter included by using all the implemented layouts established in QCA. The optimization of the proposed design made improvisation of cell count

efficiency of 34% which is about 58% in the existing work and the same kind of area reduction has presented of 43% when compared to 51%. Thus, we can implement the proposed structures for practical work. By studying analysis, we have designed a cell interaction biased ion XOR gate to implement the model of Ripple carry adder.

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