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Digital Filter Design: Novel Multiplier Realization

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Abstract

Digital filters are vital a part of digital signal process. The Finite impulse response (FIR) in various signal processing applications has been employed. It has wide range of applications such as image processing, data transmission, biomedical, wireless communication networks etc. The digital finite impulse response consists of three main blocks. They are multiplier, adder, and delay. FIR filter design causes excessive area and power consumption because of multiplications is of large number. Multiplier factor is the main block in FIR filter. Various ways are delineate within the study to execute application specific integrated circuit (ASIC) in digital finite impulse response filter. High power consumption in partial product generation of the standard multiplier factor section. In planned work, the implementation of Radix-4 Booth multiplier factor and improved booth has been performed for 16-Tap FIR filter. The multiplier factor design helps to reduce the amount of steps in multiplication and additionally in digital circuits decrease the propagation delay and the power consumption. Compared to FIR filter with traditional multiplier factor results clearly indicate that power and capacity are condensed. The results show that the improved Booth multiplier based FIR filter ends up in smallest power and space, for communication purpose and FIR filter is additionally applicable.

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Introduction

The implementation of simple and intuitive encoding or decoding has been provided by the authors of[1] in the radix-4 Booth algorithm. Proposal of adding encoder to the Booth Multiplier improves the power efficiency of Multiplication.[2] Low power consumption and high speed have established in the FIR filter styles. In FIR filter the hardware value conjointly will increase because of the rise of space. Based on the majority logic (ML), the block diagram has used a 3 input gate. It can be done using hardware also. [3] Depending on the speed of the Multiplier, the speed of the system is based. To generate the final output at the final stage, the design is implemented on software. Here the Multiplication factor matter the most.[4-7] By taking this into the consideration, the speed performance must benefit the low space FIR filter. Implementation of the FIR filter has 3 basic unit like multiplication, delay of signal and addition. Implementation of adder to the encoder in Booth multiplier has the greatest advantage as the adders adds up the result given by the encoder and decoder, which in result takes less time to give the final output and is also a power efficient one.[8] The standard multipliers in the projected work are replaced in the improved Booth number.[9-11]

FIR Filter

An FIR is a filter whose impulse response is of finite period. The designing ways of FIR filter support approximation of ideal filter. The subsequent filter approaches the proper characteristics as a result of the order of the filter will increase.[8] An FIR consists of an adder, a multiplier and delay elements.[12-23]

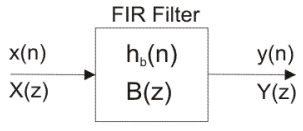

Fig. 1: Block Diagram of FIR filter

The design methodology starts with needs and specifications of the FIR filter. The strategy used within the methodology of the filter depends upon the implementation and specifications. It is very vital to elect the power technique for FIR filter, due to efficiency and ease of the FIR filter and most commonly window technique is utilized.[24-33]

FIR filters use the versions of the input that are delayed for the filtration of input to the output signal. We call fir filter as finite because we don't have any feedback loop. The output in this type of filter goes to zero independent of the input but the time when it goes back to zero depends on the input. Since the coefficient of the fir filter is symmetrical, it is called as linear phase filter.[12] Fir filters are preferred more than the IIR's due to its stability nature. The phase of the input signal in fir filter is not distorted because the fir filter is designed in such a way that it is to be linear.[13] The implementation of the fir filter is very simple and easy. Fir filters uses more memory due to the mathematical operations performed to produce filter response. Without FIR filters some filter responses cannot be implemented.[34]-[43]

Booth Multiplier

The booth multiplier algorithm is a multiplication algorithm that allows us to multiply the two signed binary integers in 2's complement, respectively. The best advantage of using this booth multiplier is, to speed up the multiplication process. The k-bit binary variety that is used as k/2 digit by Radix -4.[4]

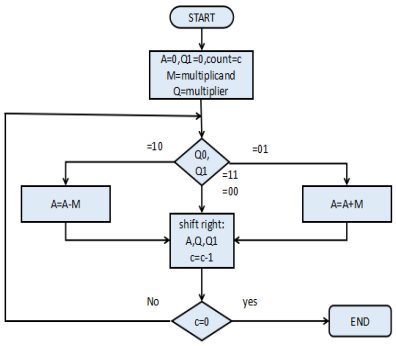

Fig. 2: Flowchart of Booth Multiplier

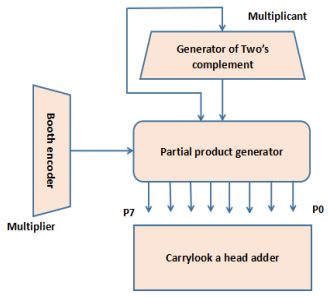

Fig. 3: Block Diagram of Booth Multiplier

To reduce the number of stages in multiplier, it performs encoding scheme. In this, one stage is little more complex than the other but they are fast. To perform multiplication it performs less no of addition operations and shift operations.

It plays an important role in integrated circuits. It is used to reduce power consumption, area occupied and delay time. It also increases scalability by modifying the modules in it. Both positive and negative multiplier uniformly. The speed is also gained by using booth multiplier. Booth multiplier helps us to increase the efficiency.

The booth multiplier algorithm is a multiplication algorithm that allows us to multiply the two signed binary integers in 2's complement respectively. The best advantage of using this booth multiplier is, to speed up the multiplication process. The k-bit binary variety that is used as k/2 digit. The disadvantage of this algorithm is for n-bit number there will be n shifts as well as additions is n/2.

Steps - Radix 2 Booth multiplications

- Let multiplicand =13 and multiplier =-6
- Converting these inputs in to binary forms. It becomes 13=1101 and 6=0110
- If there is a negative sign then perform 2's complement of that input. Then complement of 2 is 1010
- Extensions of the sign bit for the input is 13=01101 and 6=11010
- By using above table reduction of multiplier bits will takes place.
- In the Least significant bit of multiplier add 0. So it becomes 110110
- From least significant bit compare two multiplier bits so that reduction in multiplier bits takes place.
- Now -6 becomes 110110 is reduced to 0,-1, 1,-1, 0.Finally perform multiplication through product generator.
- The finally the result will be 13*-6=-78 (11110110010).

Modified Booth Algorithm

Radix-2 is having disadvantage that is for n bits n shifts are required and also n/2 additions. So it becomes more complex. To reduce the complexity improved booth re-coding algorithm is implemented. Generally modified booth algorithm consists of three parts. They are

1. Partial product generator.
2. Reduction of partial product to make rows.
3. Addition for final product.

This algorithm is used to produce high speed algorithms. Booth algorithm is comparatively slow speed so modified booth algorithm is introduced to improve the speed. This modified booths algorithm is having high speed

multiplications. Hence this is the main advantage for this algorithm. In modified booths algorithm the two things are proportional to each other they are computation time and length of operands. This is having one more advantage that is there is a reduction in area of multiplier block.

Steps for improved Booth multiplications

1. Let multiplicand = -11 and multiplier =27.
2. Multiplicand and multiplier is converted in to binary forms. Then it becomes +11=1011 and +27=11011.
3. For negative number perform 2's complement of that number. So it becomes 0101 for -11
4. Extension of the sign bit for multiplicand and multiplier is for -11= 110101 and+27=011011
5. Then perform reduction for multiplier bits.
6. In the least significant bits of multiplier add 0.
7. Take three bits LSB and compare multiplier bits and reduce multiplier bits.
8. The multiplier bit +27 (011011) is reduced to (+2,-1,-1).
9. Perform the multiplication through the product generator is reduced.
10. Final result that is -11*+27= -297(111011010111).

Proposed Booth Multiplier

4-Bit Adder

As we know that a 1 bit adder cannot add the binary numbers that are more than 1 bit, so we use the 1bit adders to implement for more than 1 bit binary numbers. We use four 1 bit adders to form a 4 bit adder.

The (Fig. 5) block diagram represents the 4 bit adder using 1 bit adders. When a 4 bit binary number is given as an input then the number is divided into single bits and send to the adder, after one block completes its operation then the carry goes to other block hence this process is flowed for the other blocks to.

Then after the structure of a 4 bit adder has been simplified so that there time taken is decreased and output is also shown quicker than before.

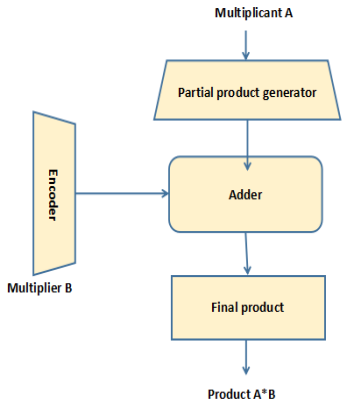

Fig. 4: Block Diagram of Modified Booth Multiplier

The figure Fig.9 represents the simplified form of the 4 bit adder. Using this 4 bit adder we can form an 8 bit adder and a 12 bit adder.

12-Bit Adder

To form a 12 bit adder, three 4 bit adders are needed. The block diagram for 12 bit adder is shown in Fig. 7.

Booth Multiplier (Fig. 8)

Experimental Validation of Proposed Designs

Simulation result of 8X3 Encoder

As seen in the above figure inputs are given and 3 outputs are shown finally. Let us consider a block i.e. block 20fs the inputs for the particular block is 0 0 0 1 0 0 0 0 and the output of that input is 0 1 1 from top to bottom. Similarly, each and every block has its own way of doing it. Mathematically we can prove the above output.

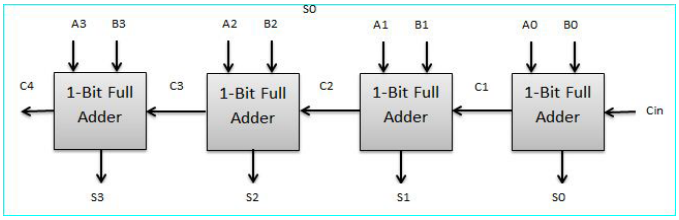

Fig. 5: Block Diagram of 4-Bit Adder using 1-Bit Adder

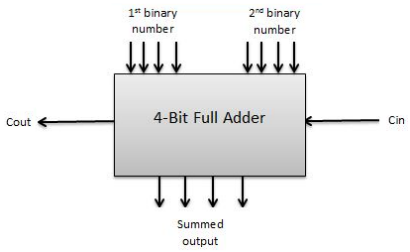

Fig. 6: Block Diagram of simplified 4-Bit Adder

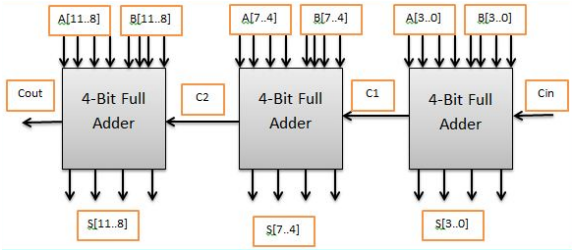

Fig. 7: Block Diagram of 12-Bit Adder

Fig. 8: Block Diagram of Proposed Booth Multiplexer

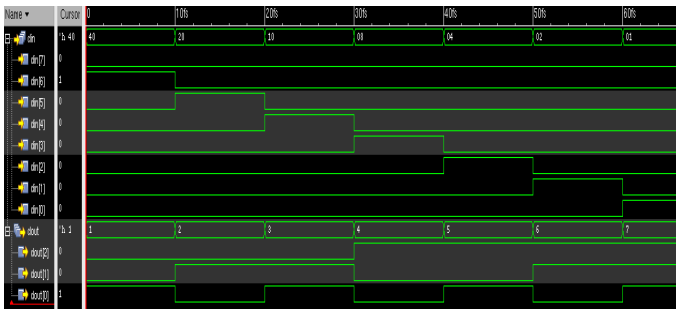

Fig. 9: Simulation result of 8X3 Encoder

The mathematical expressions for 8X3 Encoder are,

$$A2=Y7+ Y6+ Y5+ Y4 \quad (1)$$
$$A1=Y7+ Y6+ Y3+ Y2 \quad (2)$$
$$A0=Y7+ Y5+ Y3+ Y1 \quad (3)$$

'+' represents logical OR operation

Now, Here $Y_0=0$, $Y_1=0$, $Y_2=0$, $Y_3=1$, $Y_4=0$, $Y_5=0$, $Y_6=0$, $Y_7=0$. Substitute the values in the given equations (1), (2), (3), we get,

$$A_2=0+0+0+0=0$$
$$A_1=0+0+1+0=1$$
$$A_0=0+0+1+0=1$$

- In the same way all the other inputs in shown in the simulation graph can be proved.

To do a thorough check we can even see the truth table related to the 8X3 Encoder and the truth table is shown in Table 4. Similarly each and every block has its own way of doing it.

Simulation result of 3X8 Decoder

As seen in the above figure inputs are given and 8 outputs are shown finally. Let us consider a block i.e. block 50fs the inputs for the particular block are 1 0 1 and the output seen are 0 0 1 0 0 0 0 0 from top to bottom. Mathematically we can prove the above output.

The Mathematical expressions for 3X8 Decoder are,

$Y_0=X'.\ Y'.Z'$ (4); $Y_1=X'.\ Y'.Z$ (5)
Y2=X'. Y.Z' (6); Y3=X'. Y.Z (7)
Y4=X. Y'.Z' (8); Y5=X. Y'.Z (9)
Y6=X.Y.Z' (10); Y7=X. Y.Z (11)

'.' Represents logical AND operation

Now, Here $X=1$, $Y=0$, $Z=1$. Substitute the values in the above equations (1) to (8), we get,

$Y_0 = 0.\ 1\ .0 = 0$; $Y_1 = 0.\ 1\ .1 = 0$
$Y_2 = 0.\ 0\ .0 = 0$; $Y_3 = 0.\ 0\ .1 = 0$
$Y_4 = 1.\ 1\ .0 = 0$; $Y_5 = 1.\ 1\ .1 = 1$
$Y_6 = 1.\ 0\ .0 = 0$; $Y_7 = 1.\ 0\ .1 = 0$

When seen from bottom to top the order of the output mathematically is 00100000. In the similar way we can find the other outputs too. To do a thorough check we can even see the truth table related to the 3X8 Decoder and the truth table is shown in Table 6. Similarly each and every block has its own way of doing it.

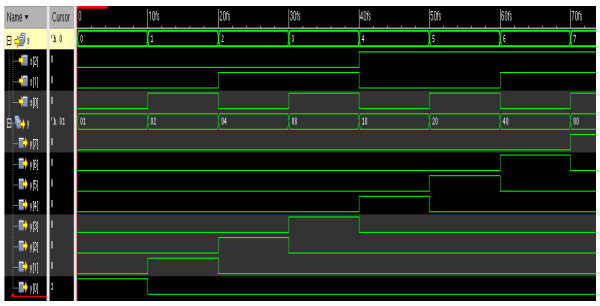

Fig. 10: A. Simulation result of 3X8 Decoder

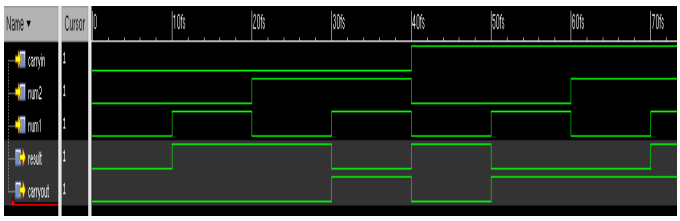

Fig. 11: Simulation result of 1-Bit Adder

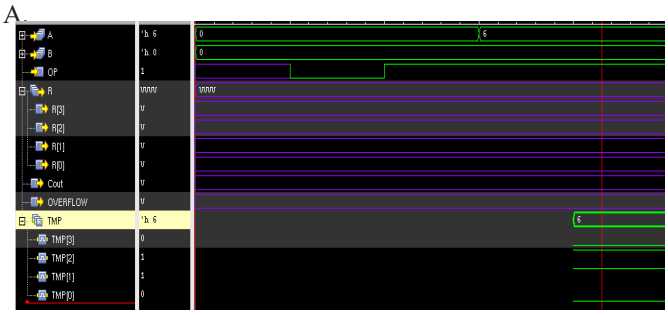

Fig. 12: Simulation result of 4-Bit Adder

Simulation result of 1-Bit Adder

As seen in the above fig inputs and a carry input is given and 2 outputs where one is the sum output and the other is the carry output. Let us consider a block i.e. block 10fs where 0 0 1 is the input and 1 0 is the output from top to bottom. We can prove it mathematically.

The Mathematical expressions of 1-Bit Adder are,

$$Sum = num_1 \oplus num_2 \oplus carry_{in} \quad (12)$$

$$Carry_{out} = (num_1 \cdot num_2) + ((num_1 \oplus num_2) \cdot carry_{in}) \quad (13)$$

' $\oplus$ ' Represents logical XOR operation

'+' Represents logical OR operation

'.' Represents logical AND operation

Now, Here $carry_{in}=0$, $num_2=0$, $num_1=1$. Substitute the above values in equation (1) & (2), we get,

$$Sum = 1 \oplus 0 \oplus 0 = 1$$
$$Carry_{out} = (1.0) \oplus ((1 \oplus 0) \cdot 0) = 0 + 0 = 0$$

To do a thorough check we can even see the truth table related to the 1-Bit Adder and the truth table is shown in Table 6. Similarly each and every block has its own way of doing it.

Simulation result of 4-Bit Adder

The result of the 4-bit Adder is based on the block diagram of it. Initially 3 inputs i.e. A_1, B_1 & C_{in} inputs are given then we get the first output sum S_0 and carry C_0. Then A_2, B_2 as second inputs and C_{in} as carry input then we get, second output sum S_1 and carry C_1. In this similar way the third and fourth outputs S_2, S_3 and carry C_2, C_3 are noted. This is the whole process only for two 4-bit binary numbers. There are many combinations related to the two 4-bit binary numbers so, for those possibilities also we need perform the same technique as mentioned above.

Conclusion

By implementing the improved booth algorithm and radix booth multiplier with 16-Tap FIR filter we can reduce power and can have high speed for the final output. The space is also reduced because of the usage of multiplier which reduces the number of steps taken therefore reducing the overall space. These are the main aims of this paper. The internal elements present in the booth multiplier are encoder, decoder and adder. These elements perform a major role in the booth multiplexing. Using the xilinx software we perform the operations based on encoder, decoder and adder. VHDL codes need to be coded for these internal elements and then after these codes are used in xilinx software so that we get, the final simulation output. The outputs of these elements are observed and been verified with their related truth table and proved by the mathematically by using their logical expressions of the internal elements i.e. encoder, decoder and adder. And can refer the simulation results.

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