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Next Generation Semiconductor based Fundamental Computation Module Implementation

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Abstract

Full adder was also known as basic component in any digital circuitry for microprocessors, digital signal processors and for every processing chip used in nowadays technology. The main purpose of full adder is to do basic logic along with operations of arithmetic's. Thus it allows designer for further advancement of the circuits with improvement in characteristic such as robust, compact, efficient, including scalabilities. Carbon Nanotube Field Effect Transistor (CNTFET) are came into use as substitute of CMOS innovation for planning circuits in the arising innovation. Main moto for this model is to design a advanced and high performable full adder circuit using CNTFET transistor admired by new CMOS full adder plan with cutting edge execution boundaries. To a voltage supply of 0.7V, the quantity of semiconductors was diminished to 10 and furthermore the force was generally separated in two differentiated to the top accessible adder that is based on CNTFET. This plan furnishes checked improvement when contrasted and the current plans like C-CMOS, TFA, TGA, HPSC, 18T-FA adder and so on. Similar information examination show that is 37%, 50%, and 49% improvement as far as territory, delay, and power delay contrasted and both CNTFET and CMOS based adders in existing plans. The circuit was planned in 20nm innovation and reenacted with CADENCE apparatuses.

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Introduction

To create a new purpose and reach growth-up expectations semiconductor technology is in constant innovational race. For consumers, industry and scientific purpose implemented semiconductor devices are predicted to provide high speed with high performance, flexibility and less power utilization. Power utilization is a key component which impact the operation of a circuit in embedded electronics product like connected watches, mobile phones and laptops.[1-14] Carbon Nano Tube Field Effect Transistor (CNTFET) was most favorable innovation that has impressive advantages. Carbon Nanotube Field Effect Transistor can easily overcome challenges such as low off-current properties and channel effects. CNTFET has best controlling over the channels formations, good threshold voltages, best sub-threshold slopes, highest electrons mobilities, high current density, highest transconductance and high linearities. In this research paper, CNTFET based full adder was created using 20nm technology.[5-8] After simulation and evaluation, this design provides an impressive PDP with less transistors.[15-28]

CNTFET Modelling

In today's technologies, CNTFET is one of the most advanced technologies because of its special physical characteristics. It also provides many advantages like quasi-ballistic transport because of its high mobility, rapid switching due to high carrier speed, for better electrostatic control almost one dimensional structure of carbon nanotube are used.[9-11] Also each carbon nanotubes respond like a channels contraries for MOSFET, and channel is made by the entire silicon. The moment of n types and p types of CNTFET are identical and same current is used for driving the two types of transistors to transfer. This allows us to create our complete logic circuit where as it is not possible by MOSFET transistors.[29-33]

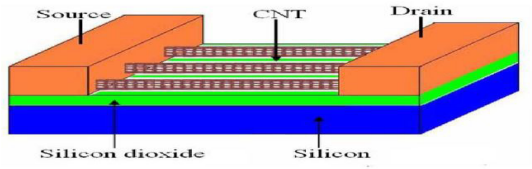

Fig. 1: CNTFET

Theoretical behavior of CNTFET

In this part, we discuss about the theoretic background which is necessary to analyze the variation effects of CNTFET technology parameters on circuit performance matrices and important device, as the CNTFET's size (width of gates), threshold voltages (V_{th}), ration of on/off currents (I_{on}/I_{off}), transconductance, slope of subthreshold (S), gate delay (td) and switching energy.[34-40]

Size of CNTFET

Pitch is known as the distances in between two of adjointed SWCNTs centers below the gate of the same CNTFET, where size of gate where device contact are impacted directly.[15] Total size of the CNTFET will be given by the gate width. By using pitch we can determine the width of the gate.[41-43]

CNTFET Threshold Voltage

For designing the circuits with best performance on an average of power consumption and the speed, it is necessary to determine the threshold voltage because that affects the speed of switching, power leakage and the current.[16-18] Similarly to a MOSFET device, a CNTFET also has threshold voltage that is the required voltage to turn ON the device through the gate electrostatically. By changing the diameter of its CNTs the threshold voltage can be adjusted and this is the greatest advantage of CNTFET. Than MOSFET the CNTFET becomes more flexible by these practical characteristics for the digital circuits design and it also makes it suitable for the multi-threshold circuits designing. CNTFETs threshold voltage is considered as the half band gap.[19]

Gate Delay

To the time that the output of the gate logic is valid and stable and the gate delay is translated as the amount of time which is starting from when the input to a logic gate becomes stable and valid. Frequently, this is related to the required time to reach 50% for the output of its final output level when there are changes in its input. The speed of a device is shown by the gate delay.[20]

Existing Methods and Analysis

In applications of digital electronics like logic gates and highly used element is MOSFET. But MOSFET based on logic gates face many problems as like others in nanotechnology. That is why it is necessary to replace and for this CNTFET based logic gates have been introduced. Over MOSFET based logic gates CNTFET based logic gates have some extraordinary advantages.[21]

Power delay product (PDP) and Sensitivity

The necessary factors that have to be considered in the circuitry of logic gates due to complexity are power consumption and power delay product (PDP) of the logic gates. Compared to the PDP of CNTFET based logic gates PDP of MOSFET based logic gates are 90-100 times greater. At low power supply PDP of CNTFET logic gates decreases and PDP of MOSFET logic gates increases. That is the reason why, in nanofabrication, the great advantage over fabrication of logic gates based on CMOS technology is low power consumption for CNTFET logic gate is occurred.[4-7]

Probability of Destroying

With rise in temperature the power delay product as well as power dissipation of MOSFET based logic gates increases, with increasing temperature the power delay product (PDP) and power dissipation remains constant in case of CNTFET based logic gates. The remarkable performance of CNTFET based logic gates against MOSFET based logic gates are shown in Fig. 3 and Fig. 4. When the temperature is high the power consumption as well as heat dissipation of MOSFET based logic gates is greater. Greater possibility of destroying the devices is caused by greater heat dissipation. At the high temperature that is the reason why the probability of destroying of MOSFET based logic gates is larger than CNTFET based logic gates.

Leakage power and Voltage gain

Leakage power is an important aspect that is to be considered in case of power dissipation. Compared with the CNTFET based logic gates the maximum leakage power of MOSFET based logic gates is much greater (about 70-80 times). So, MOSFET logic gate has higher power dissipation than that of CNTFET logic gates. On the other side, under CNTFET configuration voltage gain of inverter (NOT gate) is greater than MOSFET based inverter (NOT gate) from their frequency response which is happened nearly 3dB observed.

Designs of full adder are available in 18T that is better version of 23T adder block. These results in increasing of transistors that causes problem in speed. More power is consumed and more area is occupied if the design consists of more number of transistors. So less number of transistors are used in this proposed model. Less number of transistors results in less load capacitance values.[5] In CNTFET based full adder there is less delay and less switching power dissipation. To have final output (sum) there are five stages of inverter. Logic operations are serially performed but they are not performed simultaneously. To produce sum and count two separate

blocks are used. Speed of the circuit and consumed power are impacted strongly. To produce the signal of sum two cascaded XOR/XNOR cells and many inverters are required. To generate sum at the second stage in multiplexer-based structure [7]. By a pass-transistor based block sum and output carry are generated in parallel. This design has advantages like high-speed computation and low power consumption, but in case of high load capacitors due to its less driving capability it suffers downfalls. We propose a new CNTFET based full adder design in this context to find solutions for these problems.

Proposed Model

To calculate the sum and carry using less transistors we proposed full adder based on CNTFET transistor. From the input bits that include the previous stage carry gives the sum and carry of any full adder. The relation among the inputs bits along with outputs bit is given as

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + BC_{in} + AC_{in} \quad (2)$$

Where *A* and *B* are the input bits. *Sum*, C_{out} and C_{in} represents the carry input.

Calculation of Power consumption

Power delay product is nothing but the result of multiplication of average power consumption and maximum delay.

$$PDP = \max(delay) * P_{avg} \quad (3)$$

Where average power can be expressed as

$$P_{avg} = I_{ds} * V_D * f_c * C_{load} \quad (4)$$

I_{ds}= drain to source current
V_{dd}=supply voltage
f_c=clock frequency
C_{load}= output load capacitance

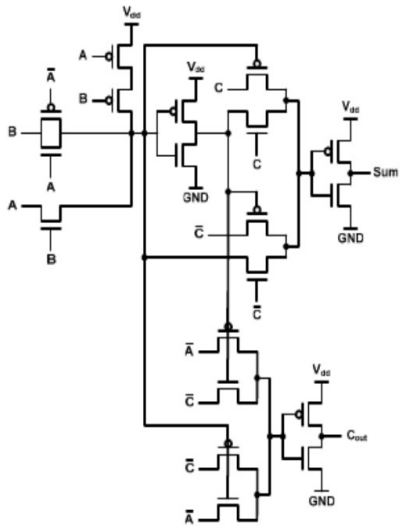

Fig. 2: 23T CNTFET Full Adder circuit

C_{load} is given by the fixed capacitance and variable capacitance as follows

$$C_{load} = C_{fix} + C_{\text{var}} \quad (5)$$

Calculation of Propagation Delay

Delay can be calculated from the time where the input signal reaches half of the V_{DD} that the output signal reaches the same level of voltage.

Advantages of Proposed model

The proposed model has high speed, Low power consumption and optimized less area.

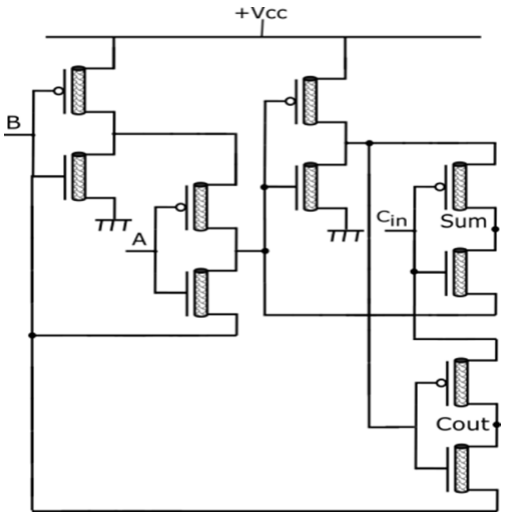

Fig. 3: The proposed full adder cell

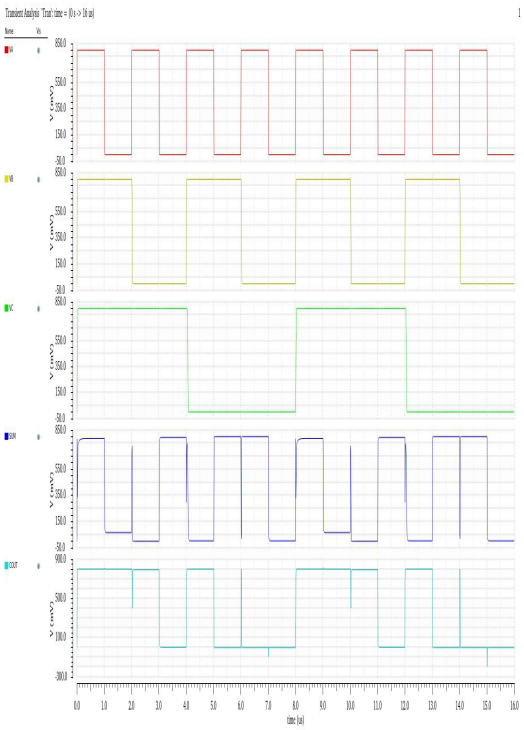

Fig. 4: Output waveforms of the proposed full adder design

Table 2: Variation of Delay, Power, PDP Vs Supply voltage (VDD)

V_{DD}	Power (µw)	Delay (ps)	PDP (aJ)
0.1	0.025	15.35	0.384
0.2	0.025	14.11	0.351
0.3	0.053	8.84	0.469
0.4	0.059	8.71	0.514
0.5	0.064	8.65	0.554
0.6	0.068	6.18	0.419
0.7	0.070	6.06	0.423
0.8	0.073	5.16	0.377
0.9	0.073	4.01	0.292
1	0.088	3.93	0.346

Applications

The applications of the proposed application are vast viz. ALU in computers and varieties of calculators; Different IC and microprocessor chips in PC and laptops; Ripple counter; important tool in DSP (Digital signal processing).

Simulation Results

By controlled transmission of the input carry signal the carry signal is generated in this design. Only through the single transmission gate the carry signal propagates. The path of the carry propagation is decreased to a considerable reduction in propagation delay. By efficient transistor sizing of strong transmission gates the delay incurred in the propagation further reduced. Power consumption and PDP are calculated.

In the table 2, the existing designs are compared with the proposed full adder.

Conclusion

A full adder cell roused from ongoing CMOS configuration has been introduced. Albeit numerous plans have been introduced as of late fully intent on lessening the quantity bought to be mulled over to make the circuit work appropriately in genuine conditions. Recreation results demonstrate that the proposed full viper shows improvement in region, deferral, and PDP by roughly 37%, half, and 49% individually contrasted with the best CNTFET-based adder found in the writing. In future work, this plan can be additionally reached out for a 32-bit full adder execution. In this current model, the carrier signals are created through controlled transmission of information carrier sign and both information flags A, B (when A=B). As carry signals spreads just from one transmitting door, the carry proliferation way are limited prompting considerable decrease in engendering delays. They brought defer about proliferation are additionally diminished from proficient semiconductor estimating of intentional consolidation solid transforming doors. In view of this data, power utilization and PDP are determined for the proposed design. Measured delay is 4ps. For 0.9 Supply the power consumption is 0.073µW and the determined PDP is 0.592 aJ.

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