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FPGA based Digital Filter Design for faster operations

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Abstract

The reduced complexity design of the IIR filter is discussed in this paper. The use of the IIR filter has been variably increasing during the present times and they are real-time applications. The filter complexity reduction is done to increase the usage of filters in FPGA. In this method, the coefficients are expressed in the form of 1's and 0's. The multiplied delays have been used which is used to scale down the complexity. Signal Flow Graph plays a critical role in identifying the difficult path. IIR Filter is programmed on basis of the Synchronous Data Flow and Pipelining. The Half Band IIR filters are used for high-performance applications. This design is processed to implement in FPGA which will result in higher speed and the cost will be variably decreased as well as the consumption of power. The entire process is implemented by using the Verilog language which reduces the complication and speeds up the whole process.

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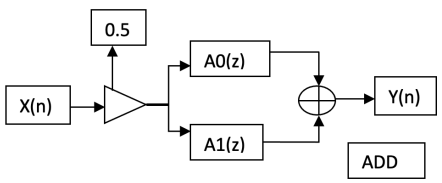
Introduction

The system which has an impulse response for a limitless amount of time is observed as Infinite Impulse Response (IIR)filter. It is one of the filter which is digital which consists of adders, Delay, MCU, SoC and processors.[1] Presently these filters are widely being used for diverse applications including communications which includes messaging, signal processing of the video and audio and etc. The digital signal processing systems which are modern have a wide number of usages for these filters.[1] When compared to the FIR filters these filters has fast computation speed and the complexity of these filters are also less. These filters work in real time and are faster compared to the others. In IIR filter, the output depends on past inputs, present inputs and previous outputs.[1-14]

The transfer function can be written as



(1)

It is unstable and consists of both poles and zeroes. It depends on previous filter, it is called Recursive Filter. It does not have a linear Phase Character. IIR filters are designed using Analog filters such as Butterworth filter, Chebyshev Filter and also the Elliptical Filter.[2]

In order to design IIR filter, we use methods such as Impulse Invariant Method, Matched Z-Transform and Bilinear Transformation. These methods are used to design Low pass IIR filters. In order to design high order IIR filter, filter stages of all pass filter, the delays and the masking filter methods.[15-32]

The frequency components of the input signals is allowed by the all pass filter which does not have any attenuation and the all pass filter will also provide different frequency of predictive phase shifts of the input signal. All Pass Filters are also named as Delay Equalizers or Phase Correctors.[3] The Amplitude of an all pass filter is unity. Phase changes from 0 degrees to 360 degrees. Applications such as Communications, when the transmission lines send the signals from one point to another point they undergo phase change. The all pass filters will be utilized to compensate the phase change.

All Pass Filters are generally used for altering the phase response of IIR filter without effecting Magnitude response. The IIR filters which are of All pass contain the properties which are beneficial which includes the number of multiplications which will be reduced, the characteristic of the phase in pass band which is highly linear and the group delay which will be cut down.[33-39]

For example we can get the IIR Filter which is of high pass from the Low Pass IIR Filter.[18], [40]

$$H_lp(z) = \frac{1*(E_0(z)+E_1(z))}{2} \quad (2)$$

$$H_hp(z) = \frac{1*(E_0(z)-E_1(z))}{2} \quad (3)$$

To implement the IIR filter based on All pass filter, is designed in MATLAB.[2]

In this paper, the implementation of is done by using a very high speed hardware description language simply known as VHDL. For FPGA the description for the application specific digital structure can be done by using VHDL.[1] It has very vast library packages. This will be used in every step of the process. The processing of the data for the mathematical equations is very effective using the VHDL language and also for calculating the frequency response and for the processing of numbers. The searching for the coefficeints and filtering the characteristics of the filter becomes faster and easier using this. When comparing to the other tools which are used for design, the VHDL provides a lot of features and the implementation will be featured in the FPGA and the optimization will be more enhancing.[2] There are many advantages to the VHDL language. Some of them are the portability which allows the which allows the description of the device to be used on other tools, the flexibility which allows the description of the code of complex logic, it is independent of any device which means that the code can be run on any device irrespective of the operating system and also it is very time efficient.[41-44]

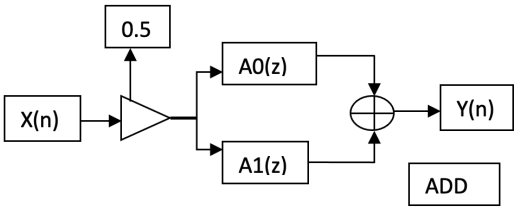


Fig. 2. All-pass Implementations of Low Pass IIR Filters

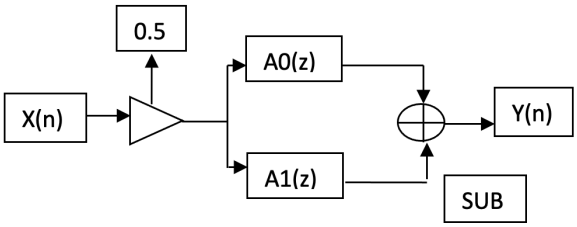


Fig. 2: All-Pass implementations of High Pass IIR filters

Introduction to FPGA

The IIR filters have been used widely and have many applications for their flexibility, the cost of the filter and speed is variably suppressed when it comes to high order filters.[2] So FPGA are implemented to achieve the results that we want to get. The Field programmable gate array which can also be referred to as FPGA. This is one of the several styles of design of the VLSI technology. These contain a huge number of the logic gates and the interconnects which are programmable. The major applications of these are in wireless communication, medicine, electronic devices etc. For the applications which are of the type of low volume they provide prototyping which is considerably very fast and also a very effective designing of the chip. These provide the sampling rate which is variably higher than those of the older versions of the DSP chips. In this the device's configuration can also be altered according to our use. In this the duration of the design is shorter which gives an advantage.[1]

The FPGA will result in many advantages to the filter and also makes the implementation easier and is mostly used to lessen the overall cost of the filter. In this the resources for the internal logic are various the configurations for applications which give high performance are magnificent. They type of the filter which is IIR filter taken in the FPGA will be concatenated. The IIR filter which is implemented using FPGA will give high throughput with efficient utilization. In this FPGA a set of coefficients will be searched for limitations of the frequency response which will be used as base.[5] The filter will be concatenated VHDL or Verilog are used to describe the model of the coefficients which are built-in which is supported by the FPGA. In several applications which include communications which require high speed FPGA is the only resolve for the IIR filter.[5]

Proposed Work

IIR filter is also developed by Frequency Response Techniques. It is used to design arbitrary-band filter and Narrow band Filter with different Specifications. Each of the delay will be changed by 'm' delays as it is the basic principle of the frequency masking.[3]

It is retrieved by connecting the periodic model filter and masking filter. FRM approach is mostly applicable for modeling the narrow band and arbitrary-band filters featuring with sharp filters with tiny word length effects.[1] Series connection of periodic model filter G(n^m) and masking filter (S(n)).[5]

$$K(n) = G(n^m).S(n) \quad (4)$$

The images produced by the G (n^m) is eliminated by masking filter. G (n^m) is obtained by G (n). This G (n) is obtained from all pass functions where

$$G(n) = Go(n) + G1(n)/2 \quad (5)$$

$$Gc(n) = Go(n) - G1(n)/2 \quad (6)$$

As the above equations state the low pass filter model for the G(n) and the other equation states the High pass complementary model filter for the Gc(n).

From the above equations G(n) is the function of the all pass filter and Gc(n) is complementary all pass function and diagrams will be same as fig 1 and fig 2.The overall filter of the transition band will be N number of times smaller when compared to the model filter. S (n) will be half band Fir filter which is a masked filter which helps in masking.[6]

It is the Magnitude Response of the Arbitrary Bandwidth IIR filter.

The Complementary Pair should satisfy the property is

$$|G(n) + Gc(n)| = 1 \quad (7)$$

The steps to design are

a. Obtain the Half Band Filter Design using Matlab Default Code (Buffer).Half Band IIR Filter is used to achieve fastness in computation, consuming of less power and miniaturization.
b. Find and Display the Coefficients of all Pass branches.
c. Define all Pass Branches and Display the Frequency response using freqz
d. Form and Compute frequency response of the equations G (n) and Gc (n).
e. Replace the delays with m and form masked FIR Filters (Fo(n) and F1(n)) which are used to remove the unwanted Spectra.

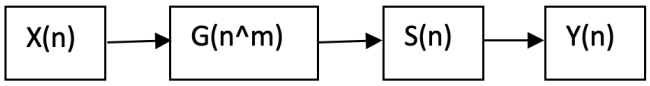


Fig. 3: Block Diagram for masking approach

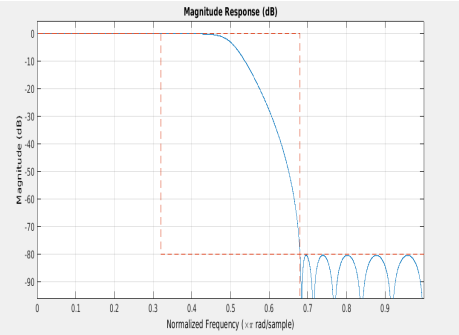


Fig. 4 IIR Filter Magnitude Response

f. Compute frequency response of

$$H(n) = G(n^m) * Fo(n) + Gc(n^m) * F1(n) \quad (8)$$

When in contrast with the FIR filters the IIR filters have minimum complexity and the effectiveness of the filtering will be greater. The usage of the FPGA system is limited and is less as its throughput is reduced and has more sensitivity due to rounding of the coefficient. Due to the path length which is critical the speed of the filter is limited to a certain amount.

The algorithm of the IIR filter is visualized by the Synchronous Data Flow which consists of coefficient multipliers, delays of the registers and the circles which are of the multipliers and adders. It consists of 4 multiplier units but only the adder and the multiplier has the crucial path.[6] The clock frequency which is maximum is very much larger in the other signal flow graphs compared to the stages of all pass and the pipelining is maximum for the signal flow graph.

In order to reduce the critical path, the multiplication to coefficient Ci in the above diagram should have minimized delay. We need to find out the Ci values. Signal Flow Graphs optimization techniques like retiming, pipelining and folding are not able to minimize the delay [4]. The integration of the filter which used the multiplied delay method and the masked filter is a complex optimization method which can't reduce the delay [1]. By replacing the multipliers which are of hardware to a different address we can improve the functionalities of the IIR filter in FPGA and also make it run a lot faster.

In order to limit the problem, a Verilog code is programmed based on Signal Flow Graph of 5th order low pass filter. Through this, we can easily implement the IIR filter in FPGA for a better pace. In order to limit the problem, a Verilog code is programmed based on Signal Flow Graph of 5th order low pass filter. Through this, we can easily implement the IIR filter in FPGA for a better pace. Pipelining is one of the technique which helps in reducing the crucial path between the input and output. In this process, it computes the time carried by the crucial path, time carried by the adders and the multipliers.

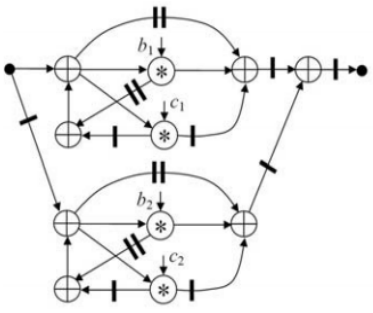


Fig. 5: SDF for Low Pass Filter of Order N=5

Table 1: Analysis of Methods

Methods	*Critical Path*	*Rate of Operation*	*Complexity*
Implementation of IIR using All pass branches and masked approaches	Critical Path is increased. It is caused due to the high delay	Due to increase in Critical Path, the speed factor is effected	In this method, we need to select the no of stages, u or m factor.it is not suitable to implement IIR filter beyond order of 10.
Implementation of programmable IIR based on SDF and pipelining.	Critical Path is reduced by using the pipelining.	The rate of operation is increased due to decrease of maximum delay between the input and output.	There is no need to choose the no of stages and m factor to construct IIR filter, so there is less complexity.

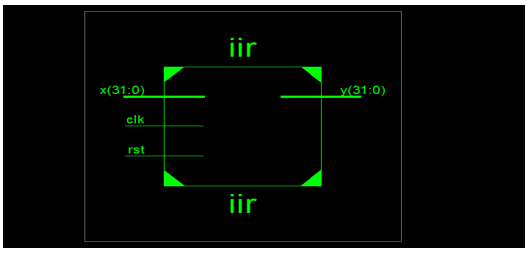


Fig. 6: Schematic View of IIR Filter

The path time must be greater than the addition of twice of adders and multipliers. Based upon that latches are introduced to reduce the delay.

Simulation Result

The figure 6 shows the schematic view of the filter which consists of the inputs and the outputs and the reset and the clock. This is the RTL design acquired from VHDL Simulator. In this filter the number of inputs and outputs are the same. In this filter the inputs are of 31 and the outputs are of 31. Additional to the input and the output the filter consists of clock and reset.

Comparative Analysis

The Table states about the filter attributes which are created based on the performance of proposed method and existing methods. Existing method is Implementation of IIR using All Pass branches and masked Approaches. Proposed method is Implementation of IIR based on SDF and Pipelining. It states about the attributes regarding the filter which are created based on the performance of filter. In the above Table, we have computation rate, critical path and the complexity of the IIR filter. As we can see from the table, the computation rate increases by a variably high amount which makes the working of the filter faster and the functionality of the filter will be very high and also the computations which are very complex can be done much faster and easier and the consumption of the power decreases which makes the device to work longer with no interruption and the main important feature the complexity of the filter is reduced by a great amount which is the main purpose of this paper.

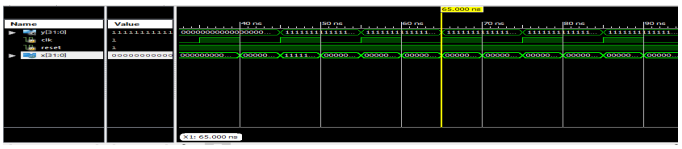


Fig. 7: Waveforms of IIR Filter

Conclusion

In this paper, it is displayed that the critical path is recovered. An IIR filter is programmed for efficient implementation in FPGA. The high-quality IIR filters can be derived from all pass sections and Masking Methods. We can gain the characteristics such as less sensitivity of the coefficients, minimal consumption of power and faster speed of computation when masking approach is performed. The problem of mapping data flow graphs(DFG) of infinite impulse response(IIR) filtering algorithms into application specific structure is considered. Methods of optimization of DFG's are considered for the purpose of finding IIR filter structures with the high throughput and hardware utilization. Optimization method is proposed which takes into account of the structural properties of FPGA, minimize it's hardware volume, and provide the designing pipelined structures with high clock frequency.

References

[1] Sergiyenko, A., Serhienko, A.: VHDL Generation of Optimized IIR Filters. In:IEEE 2nd Ukraine Conference on Electrical and Computer Engineering, UKRCON pp.1171-1174. (2019).

[2] V. Siva Nagaraju, Rapaka Anusha, and Rajeev Ratna Vallabhuni, "A Hybrid PAPR Reduction Technique in OFDM Systems," 2020 IEEE International Women in Engineering (WIE) Conference on Electrical and Computer Engineering (WIECON-ECE), Bhubaneswar, India, 26-27 Dec. 2020, pp. 364-367.

[3] S.V.S Prasad, Chandra Shaker Pittala, V. Vijay, and Rajeev Ratna Vallabhuni, "Complex Filter Design for Bluetooth Receiver Application," In 2021 6th International Conference on Communication and Electronics Systems (ICCES), Coimbatore, India, July 8-10, 2021, pp. 442-446.

[4] Chandra Shaker Pittala, J. Sravana, G. Ajitha, P. Saritha, Mohammad Khadir, V. Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Novel Methodology to Validate DUTs Using Single Access Structure," 5th International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech 2021), Kolkata, India, September 24-25, 2021, pp. 1-5.

[5] Chandra Shaker Pittala, M. Lavanya, V. Vijay, Y.V.J.C. Reddy, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Energy Efficient Decoder Circuit Using Source Biasing Technique in CNTFET Technology," 2021 Devices for Integrated Circuit (DevIC), Kalyani, India, May 19-20, 2021, pp. 610-615.

[6] Chandra Shaker Pittala, M. Lavanya, M. Saritha, V. Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Biasing Techniques: Validation of 3 to 8 Decoder Modules Using 18nm FinFET Nodes," 2021 2nd International Conference for Emerging Technology (INCET), Belagavi, India, May 21–23, 2021, pp. 1-4.

[7] P. Ashok Babu, V. Siva Nagaraju, Ramya Mariserla, and Rajeev Ratna Vallabhuni, "Realization of 8 x 4 Barrel shifter with 4-bit binary to Gray converter using FinFET for Low Power Digital Applications," Journal of Physics: Conference Series, vol. 1714, no. 1, p. 012028. IOP Publishing. doi:10.1088/1742-6596/1714/1/012028

[8] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, M. Saritha, M. Lavanya, S. China Venkateswarlu and M. Sreevani, "ECG Performance Validation Using Operational Transconductance Amplifier with Bias Current," International Journal of System Assurance Engineering and Management, vol. 12, iss. 6, 2021, pp. 1173-1179.

[9] Vallabhuni, Rajeev Ratna, M. Saritha, Sruthi Chikkapally, Vallabhuni Vijay, Chandra Shaker Pittala, and Sadulla Shaik, "Universal Shift Register Designed at Low Supply Voltages in 15 nm CNTFET Using Multiplexer," In International Conference on Emerging Applications of Information Technology, pp. 597-605. Springer, Singapore, 2021.

[10] Rajeev Ratna Vallabhuni, Jujavarapu Sravana, Chandra Shaker Pittala, Mikkili Divya, B.M.S.Rani, and Vallabhuni Vijcaay, "Universal Shift Register Designed at Low Supply Voltages in 20nm FinFET Using Multiplexer," In Intelligent Sustainable Systems, pp. 203-212. Springer, Singapore, 2022.

[11] P. Chandra Shaker, V. Parameswaran, M. Srikanth, V. Vijay, V. Siva Nagaraju, S.C. Venkateswarlu, Sadulla Shaik, and Vallabhuni Rajeev Ratna, "Realization and Comparative analysis of Thermometer code based 4-Bit Encoder using 18nm FinFET Technology for Analog to Digital Converters," In: Reddy V.S., Prasad V.K., Wang J., Reddy K.T.V. (eds) Soft Computing and Signal Processing. Advances in Intelligent Systems and Computing, vol 1325. Springer, Singapore. https://doi.org/10.1007/978-981-33-6912-2_50

[12] Rajeev Ratna Vallabhuni, G. Yamini, T. Vinitha, and S. Sanath Reddy, "Performance analysis: D-Latch modules designed using 18nm FinFET Technology," 2020 International Conference on Smart Electronics and Communication (ICOSEC), Tholurpatti, India, 10-12, September 2020, pp. 1171–1176.

[13] Rani, B.M.S, Divyasree Mikkili, Rajeev Ratna Vallabhuni, Chandra Shaker Pittala, Vijay Vallabhuni, Suneetha Bobbillapati, and Bhavani Naga Prasanna, H., "Retinal Vascular Disease Detection from Retinal Fundus Images Using Machine Learning," Australian Patent AU 2020101450. 12 Aug. 2020.

[14] Rajeev Ratna Vallabhuni, D.V.L. Sravya, M. Sree Shalini, and G. Uma Maheshwararao, "Design of Comparator using 18nm FinFET Technology for Analog to Digital Converters," 2020 7th International Conference on Smart Structures and Systems (ICSSS), Chennai, India, 23-24 july, 2020, pp. 318–323.

[15] Vallabhuni Rajeev Ratna, M. Saritha, Saipreethi. N, V. Vijay, P. Chandra Shaker, M. Divya, and Shaik Sadulla, "High Speed Energy Efficient Multiplier Using 20nm FinFET Technology," Proceedings of the International Conference on IoT Based Control Networks and Intelligent Systems (ICICNIS 2020), Palai, India, December 10-11, 2020, pp. 434-443. Available at SSRN: https://ssrn.com/abstract=3769235 or http://dx.doi.org/10.2139/ssrn.3769235

[16] Rajeev Ratna Vallabhuni, S. Lakshmanachari, G. Avanthi, and Vallabhuni Vijay, "Smart Cart Shopping System with an RFID Interface for Human Assistance," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), Thoothukudi, India, 2020, pp. 165-169, doi: 10.1109/ICISS49785.2020.9316102.

[17] Saritha, M., Kancharapu Chaitanya, Vallabhuni Vijay, Adam Aishwarya, Hasmitha Yadav, and G. Durga Prasad, "Adaptive And Recursive Vedic Karatsuba Multiplier Using Non Linear Carry Select Adder," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 22-29.

[18] V. Siva Nagaraju, P. Ashok babu, B. Sadgurbabu, and Rajeev Ratna Vallabhuni, "Design and Implementation of Low power FinFET based Compressor," 2021 3rd International Conference on Signal Processing and Communication (ICPSC), Coimbatore, India, 13-14 May 2021, pp. 532-536.

[19] P. Ashok Babu, V. Siva Nagaraju, and Rajeev Ratna Vallabhuni, "Speech Emotion Recognition System With Librosa," 2021 10th IEEE International Conference on Communication Systems and Network Technologies (CSNT), Bhopal, India, 18-19 June 2021, pp. 421-424.

[20] P. Ashok Babu, V. Siva Nagaraju, and Rajeev Ratna Vallabhuni, "8-Bit Carry Look Ahead Adder Using MGDI Technique," IoT and Analytics for Sensor Networks, Springer, Singapore, 2022, pp. 243-253.

[21] Dr. S. Selvakanmani, Mr. Rajeev Ratna Vallabhuni, Ms. B. Usha Rani, Ms. A. Praneetha, Dr. Urlam Devee Prasan, Dr. Gali Nageswara Rao, Ms. Keerthika. K, Dr. Tarun Kumar, Dr. R. Senthil Kumaran, Mr. Prabakaran.D, "A Novel Global Secure Management System with Smart Card for IoT and Cloud Computing," The Patent Office Journal No. 06/2021, India. International classification: H04L29/08. Application No. 202141000635 A.

[22] Nalajala Lakshman Pratap, Rajeev Ratna Vallabhuni, K. Ramesh Babu, K. Sravani, Bhagyanagar Krishna Kumar, Angothu Srikanth, Pijush Dutta, Swarajya Lakshmi V Papineni, Nupur Biswas, K.V.S.N.Sai Krishna Mohan, "A Novel Method of Effective Sentiment Analysis System by Improved Relevance Vector Machine," Australian Patent AU 2020104414. 31 Dec. 2020

[23] Vijay, Vallabhuni, Kancharapu Chaitanya, Chandra Shaker Pittala, S. Susri Susmitha, J. Tanusha, S. China Venkateshwarlu, and Rajeev Ratna Vallabhuni, "Physically Unclonable Functions Using Two-Level Finite State Machine," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 33-41.

[24] B. M. S. Rani, Vallabhuni Rajeev Ratna, V. Prasanna Srinivasan, S. Thenmalar, and R. Kanimozhi, "Disease prediction based retinal segmentation using bi-directional ConvLSTMU-Net," Journal of Ambient Intelligence and Humanized Computing, 2021, pp. 1-10. https://doi.org/10.1007/s12652-021-03017-y

[25] Rajeev Ratna Vallabhuni, A. Karthik, CH. V. Sai Kumar, B. Varun, P. Veerendra, and Srisailam Nayak, "Comparative Analysis of 8-Bit Manchester Carry Chain Adder Using FinFET at 18nm Technology," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), Thoothukudi, India, 2020, pp. 1579-1583, doi: 10.1109/ICISS49785.2020.9316061.

[26] R. R. Vallabhuni, P. Shruthi, G. Kavya and S. Siri Chandana, "6Transistor SRAM Cell designed using 18nm FinFET Technology," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), Thoothukudi, India, 2020, pp. 1584-1589, doi: 10.1109/ICISS49785.2020.9315929.

[27] Rajeev Ratna Vallabhuni, J. Sravana, M. Saikumar, M. Sai Sriharsha, and D. Roja Rani, "An advanced computing architecture for binary to thermometer decoder using 18nm FinFET," 2020 Third International Conference on Smart Systems and Inventive Technology (ICSSIT), Tirunelveli, India, 20-22 August, 2020, pp. 510–515.

[28] Rajeev Ratna Vallabhuni, K.C. Koteswaramma, B. Sadgurbabu, and Gowthamireddy A, "Comparative Validation of SRAM Cells Designed using 18nm FinFET for Memory Storing Applications," Proceedings of the 2nd International Conference on IoT, Social, Mobile, Analytics & Cloud in Computational Vision & Bio-Engineering (ISMAC-CVB 2020), 2020, pp. 1-10.

[29] Vijay, Vallabhuni, M. Sreevani, E. Mani Rekha, K. Moses, Chandra S. Pittala, KA Sadulla Shaik, C. Koteshwaramma, R. Jashwanth Sai, and Rajeev R. Vallabhuni, "A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 27-32.

[30] Vijay, Vallabhuni, Chandra S. Pittala, A. Usha Rani, Sadulla Shaik, M. V. Saranya, B. Vinod Kumar, RES Praveen Kumar, and Rajeev R. Vallabhuni, "Implementation of Fundamental Modules Using Quantum Dot Cellular Automata," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 12-19.

[31] Vijay, Vallabhuni, Chandra S. Pittala, K. C. Koteshwaramma, A. Sadulla Shaik, Kancharapu Chaitanya, Shiva G. Birru, Soma R. Medapalli, and Varun R. Thoranala, "Design of Unbalanced Ternary Logic Gates and Arithmetic Circuits," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 20-26.

[32] Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, Vallabhuni Vijay, Usha Rani Anam, Kancharapu Chaitanya, "Numerical analysis of various plasmonic MIM/MDM slot waveguide structures," International Journal of System Assurance Engineering and Management, 2022.

[33] M. Saritha, M. Lavanya, G. Ajitha, Mulinti Narendra Reddy, P. Annapurna, M. Sreevani, S. Swathi, S. Sushma, Vallabhuni Vijay, "A VLSI design of clock gated technique based ADC lock-in amplifier," International Journal of System Assurance Engineering and Management, 2022, pp. 1-8. https://doi.org/10.1007/s13198-022-01747-6

[34] Chandra Shaker Pittala, Vallabhuni Vijay, B. Naresh Kumar Reddy, "1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications," Silicon, 2022. https://doi.org/10.1007/s12633-022-02016-8.

[35] Vallabhuni Vijay, Kancharapu Chaitanya, T. Sai Jaideep, D. Radha Krishna Koushik, B. Sai Venumadhav, Rajeev Ratna Vallabhuni, "Design of Optimum Multiplexer In Quantum-Dot Cellular Automata," International Conference on Innovative Computing, Intelligent Communication and Smart Electrical systems (ICSES -2021), Chennai, India, September 24-25, 2021.

[36] S. China Venkateswarlu, N. Uday Kumar, D. Veeraswamy, and Vallabhuni Vijay, "Speech Intelligibility Quality in Telugu Speech Patterns Using a Wavelet-Based Hybrid Threshold Transform Method," International Conference on Intelligent Systems & Sustainable Computing (ICISSC 2021), Hyderabad, India, September 24-25, 2021.

[37] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Low power based optimal design for FPGA implemented VMFU with equipped SPST technique," National Conference on Emerging Trends in Engineering Application (NCETEA-2011), India, June 18, 2011, pp. 224-227.

[38] S. China Venkateswarlu, Ch. Sashi Kiran, R.V. Santhosh Nayan, Vijay Vallabhuni, P. Ashok Babu, V. Siva Nagaraju, "Artificial Intelligence Based Smart Home Automation System Using Internet of Things," The Patent Office Journal No. 09/2021, India. Application No. 202041057023 A.

[39] Bandi Mary Sowbhagya Rani, Vasumathi Devi Majety, Chandra Shaker Pittala, Vallabhuni Vijay, Kanumalli Satya Sandeep, Siripuri Kiran, "Road Identification Through Efficient Edge Segmentation Based on Morphological Operations," Traitement du Signal, vol. 38, no. 5, Oct. 2021, pp. 1503-1508.

[40] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Optimal design of VLSI implemented Viterbi decoding," National conference on Recent Advances in Communications & Energy Systems, (RACES-2011), Vadlamudi, India, December 5, 2011, pp. 67-71.

[41] Katikala Hima Bindu, Sadulla Shaik, V. Vijay, "FINFET Technology in Biomedical-Cochlear Implant Application," International Web Conference on Innovations in Communication and Computing, ICICC '20, India, October 5, 2020.

[42] V. Vijay, J. Prathiba, S. Niranjan Reddy, V. Raghavendra Rao, "Energy efficient CMOS Full-Adder Designed with TSMC 0.18µm Technology," International Conference on Technology and Management (ICTM-2011), Hyderabad, India, June 8-10, 2011, pp. 356-361.

[43] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, and Nakka nikhil, "Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology," VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.

[44] Vallabhuni Vijay, and Avireni Srinivasulu, "A Novel Square Wave Generator Using Second Generation Differential Current Conveyor," Arabian Journal for Science and Engineering, vol. 42, iss. 12, 2017, pp. 4983–4990.