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Machine Learning Dependent Arithmetic Module Realization for High-Speed Computing

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Abstract

Since last few years, the tiny size of MOSFET, that is less than tens of nanometers, created some operational problems such as increased gate-oxide leakage, amplified junction leakage, high sub-threshold conduction, and reduced output resistance. To overcome the above challenges, FinFET has the advantages of an increase in the operating speed, reduced power consumption, decreased static leakage current is used to realize the majority of the applications by replacing MOSFET. By considering the attractive features of the FinFET, an ALU is designed as an application. In the digital processor, the arithmetic and logical operations are executed using the Arithmetic logic unit (ALU). In this paper, power efficient 8-bit ALU is designed with Full adder (FA) and multiplexers composed of Gate diffusion input (GDI) which gained designer's choice for digital combinational circuit realization at minimum power consumption. The design is simulated using Cadence virtuoso with 20nm technology. Comparative performance analysis is carried out in contrast to the other standard circuits by taking the critical performance metrics such as delay, power, and power delay product (PDP), energy-delay product (EDP) metrics into consideration.

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Introduction

The Very Large Scale Integration (VLSI) is the task of designing an Integrated circuit by clubbing thousands of transistors into one chip. The VLSI turned up in the year 1970 when the complex Semiconductor and Communication technologies were being emerged. The electronics industry achieved a considerable expansion over the last few decades, mainly because of the rapid promotions in the large scale integration technologies and the applications of system design. With the advantages of the VLSI designs, the implementation of ICs in communications, video and image processing has been rising. Even for no portable devices, power consumption is an essential criterion due to raising in the packaging and cooling costs along with reliability issues. Considering these problems, the primary challenge for the design engineers is inadequate, realization within a targeted power without compromising the performance requirement.[1-13]

The tiny size of the MOSFET, less than tens of nanometers, created some operational problems such as high sub-threshold conduction which means; in the MOSFET, the applied voltage to gate terminal is to be decreased to maintain the reliability.[2-3] Then the threshold voltage which is to be applied to the MOSFET must also be reduced. As this threshold voltage is decreased possibly to a very great extent, the transistor will not be able to switch from the complete turn-off to complete turn-on state and vice versa. The rise of gate-oxide leakage refers to the gate oxide, serving as an insulator in between the channel and gate must be designed as thin as possible in order to elevate the conductivity of the channel and performance of the device when it is in ON state and to decrease the subthreshold leakage during OFF state of the device. The increased junction leakage means the design of junction becomes quite more difficult in smaller devices, leading to higher doping levels which lead to drain induced barrier lowering. And many more drawbacks such as lower output resistance, lower transconductance.[14-24]

The scaling of gate lengths to very short distances is possible with FinFET technology. FinFET-DGCMOS and

conventional CMOS fabrication are similar to one another, except negligible disturbances, allows the participation of more efforts in the significant involvement of the yielding the applications. FinFET channel is a un-doped structure of smaller in size portion which is placed in a perpendicular direction to that of substrate terminal. Coulomb scattering is eliminated by un-doped channel because of faster mobility in FinFETs by the unwanted impurities.[4] The two gates of the FinFET are provided to control the short channel effects without aggressively scaling down the gate-oxide thickness and increasing the channel doping density. In terms of the structure of FinFET, it is a double gate device, and the gates are formed at the vertical side of the fin using a thin gate oxide layer. Fin is a thin layer between the source and drain. FinFET reduces the levels of the leakage current and mitigates the short channel effects.[5] In this paper, the reduction in power consumption by scaling down the size of a transistor in nanoelectronics with the help of FinFET is achieved.

This paper mainly focuses on the implementation of 8-bit ALU using FinFET with 20nm technology. ALU is the core part of the central processing unit and is a combinational digital electronic circuit which accomplishes all the logical and arithmetic operations. Arithmetic modules provide minimum energy consumption at extended reliability plays a crucial role in the die. Thereby, the design changes in the ALU reflect a significant effect on the overall performance of the whole processor. To meet the reduced energy consumption and increased speed of ALU, designs require arithmetic, circuit and system level methodologies involvement.[6] Even much of the logic styles viz. clock gating, frequency, and voltage scaling are producing the minimum power consumption applications, but few amongst those are offering improved power consumption factor with the optimized die size.[25-33]

The emerging features in the new era of integrated circuit (IC) are driven with the modern days' technological advancements in the processing of silicon technology. With the revolutionary change in the realization of commercial ICs, the chip development foundries are producing the highly complex, enhanced reliability, minimum energy consumption, and more robustness processors. The central processing unit (CPU) is the basic module inside the microprocessor and composed with the ALU as a primary module. The key operations of the ALU are both arithmetic and logical operations. The arithmetic operations of addition, subtraction, multiplication and division are performed as addition, inverted addition, recursive addition, and recursive inverted addition, respectively. The majority of the addition operations in the digital system are formed using the full adder, and the major constraint in the full adder design is to produce the circuits with minimum energy dissipation, less delay, energy efficiency in addition to reliability feature [8]. In contrast to the existed MOSFET designs, the novel innovation of FinFET models is considered to implement the full adder with the improved parameters of both device and energy efficiency. The 8-bit ALU is developed using Full adder and Multiplexers which are composed by using gate diffusion input (GDI) technique [34]-[39].

The remaining paper is organized as follows: The FinFET characteristics and modeling are discussed in section II concerning their structural behavior. Section III elaborated the design of proposed 8 bit ALU blocks using FinFET spectre models in cadence virtuoso environment. The functional verification of the constructed circuits has presented in section IV with the relevant simulation results. And finally, the conclusion is given in section V regarding the fulfillment of primary objectives.

FinFET Characteristics and Modeling

FinFET has got the name as such because of the Field effect transistor (FET) with a structure that view as a set of fins when gazed. It consists of a conducting region, which mainly surrounded with the thin 'fin' structure and is built on silicon on insulator by which the name 'FinFET' is evolved. The device channel for effective conduction is calculated with the fin thickness.

The FinFET is a non-planar device; double gate transistor, which is either a bulk Silicon-On-Insulator (SOI) or on Silicon Wafers [2]-[9]. This is importantly based on single gate transistor design. There are two different types of FinFET. They are Bulk FinFET and SOI FinFET. The critical characteristic of the FinFET is that it has a conducting channel that is bounded by a thin silicon fin [10]. This mainly forms the body of the device. These fins are nothing but the channel between the source and drain. The gate terminal is bounded around the channel. This lets the formation of the several gate electrodes to reduce the leakage current and to improve the drive current [11]-[12].

The FinFET works the same as that of Conventional MOSFET. It operates in two modes: Enhancement mode and Depletion mode. The working characteristics are identical in both modes, but the only difference is that, in the enhancement mode, if no voltage is given to the gate terminal, it doesn't conduct whereas in the depletion

(a) Shorted Gate FinFET ($V_{fg} \neq V_{bg}$) (b) Independent Gate ($V_{fg} \neq V_{bg}$)

Fig. 1: FinFET Models

mode, if the voltage is applied to the gate, it doesn't conduct. In the enhancement mode when the voltage is applied to the gate terminal, a parallel plate capacitor is formed. The gate is made up of the oxide layer. The surface below the oxide layer is located between the source and drain. When a small amount of positive voltage is applied to the gate concerning the source, a depletion region is formed. This region is reversed to n-type by the applied positive voltage. Then a region is formed at the interface between Si and SiO2. This applied positive voltage attracts the electrons from the source terminal to the drain terminal. By this, an electron reach channel is formed. The flow of current starts by applying a voltage between the source and drain. This flow of current is dependent on the voltage applied to the gate.

The advantages and applications of FinFET are, it consumes very less power that allows higher integration levels [13]. It operates at the lower voltages as the threshold voltage given is less. The FinFET has passed the barrier of 20nm which was previously a barrier. The static leakage current has been reduced up to 90% when compared to that of traditional methods, and its operational speed has been increased up to 30% than non FinFET devices. Samsung Electronics has incorporated FinFET in its 14nm process. Along with Samsung, Apple, Intel and Taiwan Semiconductor Manufacturing Company (TSMC) are set to ship the 14nm technology, which is a benefit to all smartphones as it will speed with the phone.

Proposed 8 bit ALU Block Using FinFET Models

Apart from the traditional CMOS design, the GDI technique is another low power and area efficient technique [14]. The aim of the GDI technique is to improve the performance of logic circuits [15]. A common GDI cell comprises of four terminals. They are P (PMOS outer diffusion node), G (Common gate input for both PMOS and NMOS transistors), D (Common diffusion for both the transistors), N (NMOS outer diffusion node).

GDI based Multiplexer

GDI based logic is used to implement 2:1 MUX whose function is based on the use of a simple cell (Figure 2). When the select line is fed with '0' the output will be the data 'A.' And when select line is fed with '1' the output will be the data 'B' (Table 1). The below truth table shows the functionality of the 2x1 Multiplexer.

GDI based logic is to implement 4:1 MUX whose function is based on the use of a simple cell. When the select line S0 is fed with '0' the output will be the data 'A' or 'C.' And when select line S1 is fed with '1' the output will be the data 'B' or 'D.' The below table 2 shows the functionality of 4x1 MUX.

11T Full Adder

A full adder is a fundamental requisite to design an ALU. The 11T methodology is used for developing Full Adder; this is another way of designing Full Adder to reduce power and delay. Full Adder is depicted in Fig. 4. This circuit operates at very low voltages such as less than 1V. This circuit is driven with a supply voltage of 0.9 (Vdd). The Input A is given to the gate of the terminal of p1, n1 and drain terminal of p2. Input B is applied to the gate terminals of the transistors p2 and n2 and the drain terminal of the n1. The passage of the signal occurs from gate to drain terminal during the ON condition of, and it became possible when the applied voltage (Vs) is higher to that of threshold voltage (Vth). That means the voltage is passed from gate to drain. So, when the Input A is high, it gives the signal applied to the terminal B. Full Adder is built using low power EX-OR gates and 2×1 Multiplexer. The outputs of 'Sum' and 'carry' (Cout) are obtained from EX-OR and Multiplexer circuits, respectively. Additional transistor numbered as n6 takes minimum power as it is driven with the ultra-low mode in combination with the

Table 1: The truth table of 2x1 Multiplexer

Select line	$V_0 = \overline{S_0}A + S_0B$
S0	Y
0	A
1	B

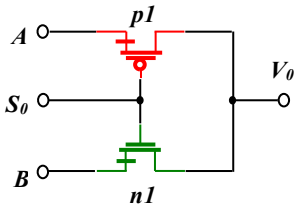


Fig. 2: 2x1 Multiplexer

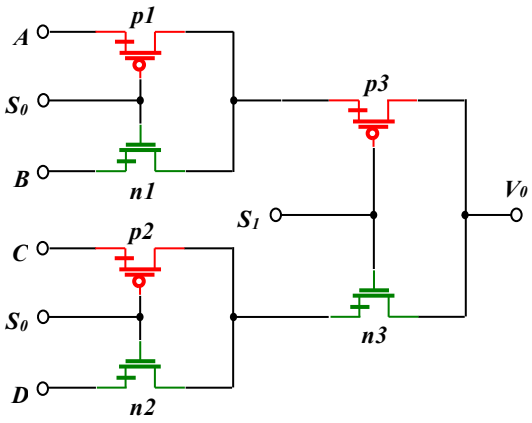


Fig. 3: 4x1 Multiplexer

sub-threshold current. The voltage across the gate to source (VGS) become higher to that of threshold voltage (VTH) because of strong inversion region, and this leads to accumulating minority charge carriers by vanishing the majority charge carriers. The subthreshold current being generated because of leakage current by the deployment of minority charge carriers during the case of the weak inversion region of VTH is greater than VGS. The required operation of the circuit is met with sufficient current which is gained from the subthreshold current at VDD value is lower than the VTH. The resultant current gives the circuit to operate with ultra-low mode by consuming minimum power. Successful operation of 11T full adder is achieved with an additional transistor, n6 at the subthreshold mode Table 3.

1-Bit & 8- Bit ALU

For any input over the input terminals A, B and C the ALU perform arithmetic and logical operations depending on the input given over the select line (Table 4). The ALU is a part of the processor that tackles all the arithmetic and logical operations as it is named. The above truth table shows the operations performed by the ALU depend on 3 Bit select line giving eight conditions. Let the input A is driven with logical '0', B with logical '1' and C with logical '1'. The Logical AND operation is performed when the select line S2 is fed with logical '0', S1 logical '0' and S0 as logical '0'. The ALU is INCREMENTED from its present state when the select line S2 is driven by logical '0', S1 with logical '0' and S0 logical '1'. The operation Logical OR is implemented when S2 is fed with logical '0', S1 logical '1' and S0 as logical '0'. DECREMENT operation is carried out when select line S2 is fed with logical '0', S1 logical '1' and S0 with logical '1'. The SUBTRACTION operation turns up for the applied signal over select line S2 is logical '1', S1 is logical '0', S0 is logical '0'. For the Logical EX-OR operation the select line S2 is to be fed with logical '1', S1 logical '0' and S0 logical '1'. The Logical EX-NOR operation is accomplished when the select line S2 is fed with logical '1', S1 with logical '1' and S0 with a logical '0'. That which is last, the ADDITION operation is carried out for S2 is fed with logical '1', S1 with logical '1' and S0 with logical '1'.

Table 2: The truth table of 4x1 Multiplexer

Select line		*Output*
S_0	S_1	$V_0 = \overline{S_0}\overline{S_1}A + \overline{S_0}S_1B + S_0\overline{S_1}C + S_0S_1D$
0	0	A
0	1	C
1	0	B
1	1	D

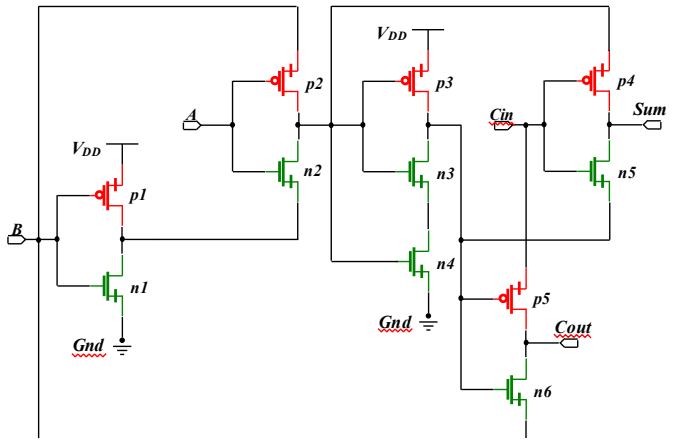


Fig. 4: Block Diagram of 1-Bit ALU [16].

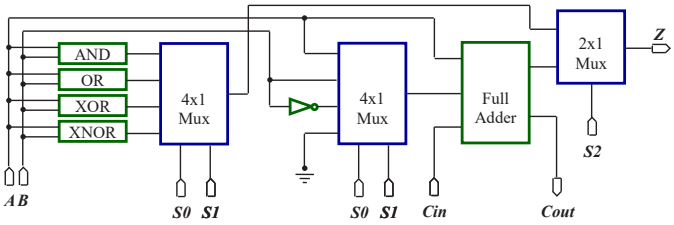


Fig. 5: Block Diagram of 8-Bit ALU

Table 3: The truth table of 11T Full Adder

Input			*Output*	
A	*B*	*Cin*	*Sum*	*Cout*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4: 1-Bit ALU for the Inputs A=0, B=1, and C=1

Select Lines				
S2	*S1*	*S0*	*Operation*	*Output*
0	0	0	AND	0
0	0	1	INCREMENT	1
0	1	0	OR	1
0	1	1	DECREMENT	0
1	0	0	SUBTRACTION	1
1	0	1	XOR	0
1	1	0	SUBTRACTION	0
1	1	1	ADDITION	1

For the 8-Bit ALU shown in Fig. 6, A, B, and C are Inputs of ALU. S0, S1 as S2 are 3-bit selection lines. F0 and F1 are Output of 1-bit ALU. F14 is the output of 8-Bit ALU, and F15 is carry obtained for last Full adder.

For any input over the input terminals A, B, and C, the ALU performs arithmetic and logical operations depending on the input given over the select line. The 8-bit ALU is obtained by cascading all 1-Bit ALU's [17]-[18]. The above block diagram shows the cascaded form of all 1-Bit ALU's. The carry which is obtained for the first Full adder's ALU is forwarded to the next Full adder's ALU. This process is continued to last ALU to form an 8-bit ALU.

Simulation Results and Experimental Findings of the Proposed Work

The circuit is shown in Fig. 2 and Fig. 3 are simulated using the Cadence virtuoso tool by considering the FinFET technology spectre files. The voltage applied to the proposed circuit is 600mv or 0.6 V which falls under the operating voltage range of the FinFET. The multiplexers are designed using Gate Diffusion Input (GDI) technique which is advantageous in the field of reducing the circuit area and the supply voltage. The output (Vout) is obtained depending on the selection lines (Vs), (Vs0) and (Vs1) for both the multiplexers. When (Vs) is given with 0V the input 'A' is passed to the output and when (Vs) is given with 0.6 V then 'B' is passed to the output. Similarly, when (Vs0) is applied with 0 V the input 'A' and 'C' are passed to the next level, for (Vs1) when applied with 0.6 V, input 'B' and 'D' is passed to the next level. Depending on data over terminal Vs1 the inputs 'A', 'B,' 'C' or 'D' as passed over the output terminal. The simulated output of Fig. 2 and Fig. 3 are shown in Fig. 7 and Fig. 8, respectively.

Full Adder using 11T is shown in Fig. 4. Is simulated using the Cadence Virtuoso tool by considering the FinFET technology spectra files. Moreover, its simulated output is shown in Fig. 9. The 11T Full Adder operates in ultra-low mode by consuming minimum power. The voltage applied to the proposed circuit is 600mv or 0.6 V. The Full Adder is responsible for the three-bit addition, whereas Half Adder can only add two bits and neglects the carry which

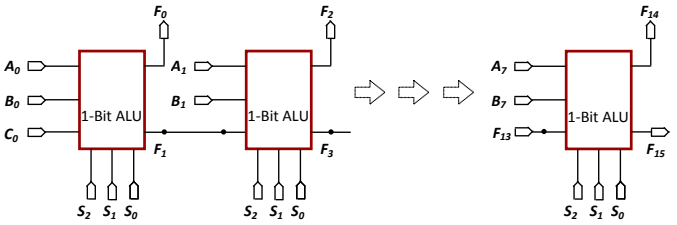


Fig. 6: Block Diagram of 8-Bit ALU

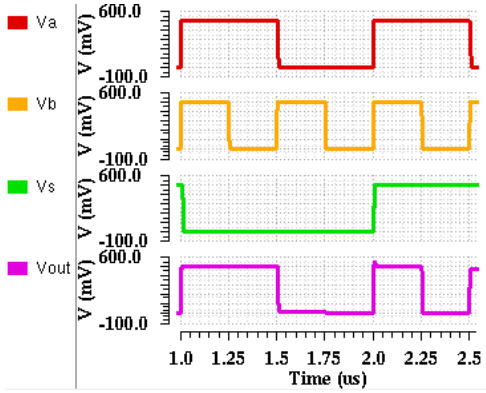


Fig. 7: Simulated Response of 2x1 MUX shown in Fig. 2

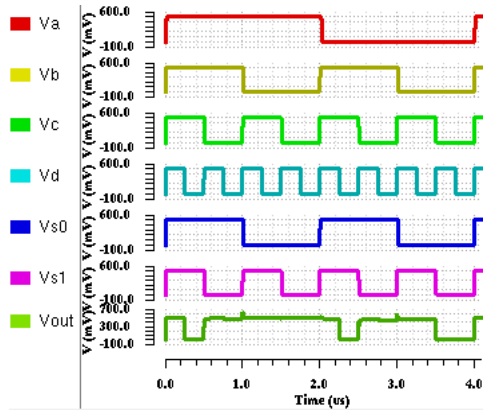


Fig. 8: Simulated Response of 4x1 MUX shown in Fig. 3.

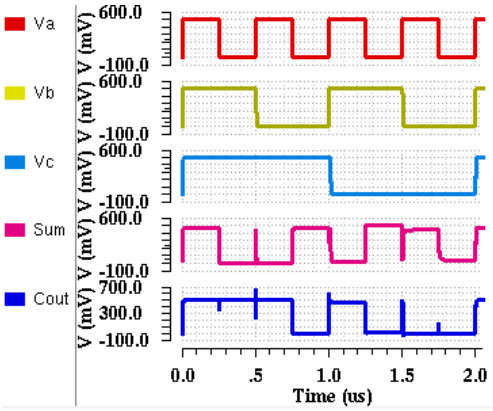


Fig. 9: Simulated Response of 11T Full Adder shown in Fig. 4.

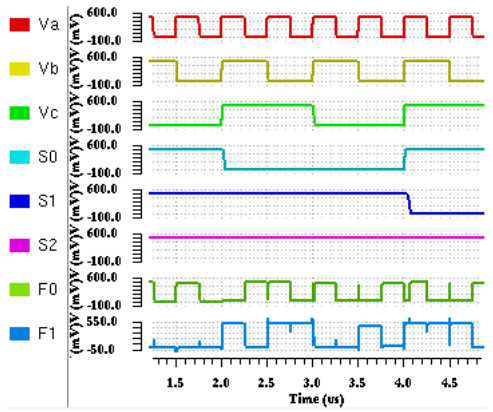
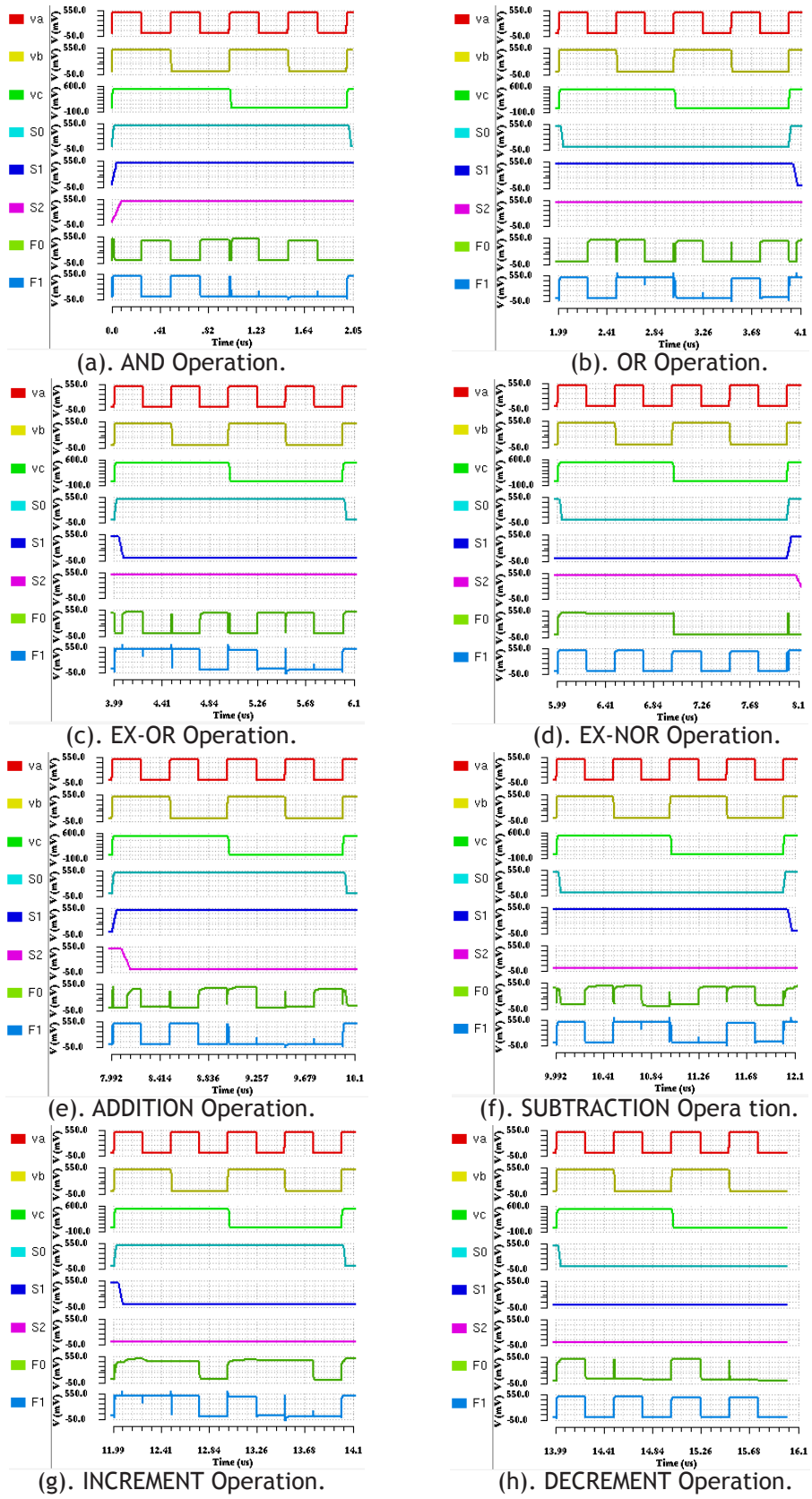


Fig. 10: Simulated Response of 1-Bit ALU shown in Fig. 5.

is obtained. The input (Vc) is added along with the bits with (Va) and (Vb) which is the carry output obtained from the circuit itself.

The simulation of 1-Bit ALU shown in Fig. 5. is carried out and the simulated output is depicted in Fig. 10. The proposed circuit operates with a voltage of 0.6 V or 600mv.



(a). AND Operation. (b). OR Operation.

(c). EX-OR Operation. (d). EX-NOR Operation.

(e). ADDITION Operation. (f). SUBTRACTION Opera tion.

(g). INCREMENT Operation. (h). DECREMENT Operation.

Fig. 11: Simulated Response of 1-Bit ALU shown in Fig. 6

Table 5: Analysis of Power, Delay, PDP and EDP.

Design	Power	Delay	PDP	EDP
Full adder	3.6nW	4.4ps	15.84nW*ps	69.6J* nW*ps
GDI based 2×1 MUX	9.9nW	9.9nW	12.87nW*ps	16.731J* nW*ps
GDI based 4×1 MUX	19nW	19nW	153.9nW*ns	1246.59J* nW*ns
1-Bit ALU	26.8nW	2.17ns	58.15nW*ns	126.198J* nW*ns
8-Bit ALU	0.2μW	1.97ns	0.394μW*ns	0.776J* μW*ns

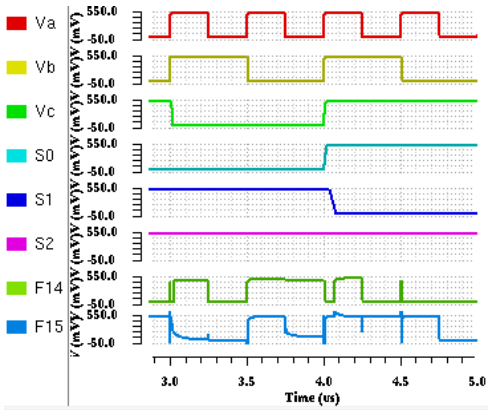


Fig. 12: Transient Response of 8-Bit ALU shown in Fig.6

The response consists of eight different operations, which are the combination of arithmetic and logical operations and these operations depend on the input given over the selection lines (S0), (S1) and (S2). The (F0) is the output of the 1-Bit ALU as shown in Fig. 10. and (F1) is the input which is applied to the ALU during cascading.

The above are the transient responses of 8 individual operations performed by the 1-Bit ALU. The ALU yields eight different operations in which four are arithmetic, and four are logical operations depending on the select line. The sub-figures in Fig. 11. shows the different operations of the 1-Bit ALU for the supply voltage of 0.6V. The role of selection line which is about three bit plays a vital role in delivering the output responses which are as follows.

The Fig. 11 (a) shows, Logical AND operation when the select line S2 is fed with logical '0', S1 logical '0' and S0 as logical '0'. The ALU is INCREMENTED from its present state when the select line S2 is driven by logical '0', S1 with logical '0' and S0 logical '1' as shown in Fig. 11 (g). The Logical OR Operation as shown in (b) is implemented when S2 is fed with logical '0', S1 logical '1' and S0 as logical '0'. The DECREMENT operation is carried out when select line S2 is fed with logical '0', S1 logical '1' and S0 with logical '1' as depicted in Fig. 11 (h). As shown in Fig. 11 (f) SUBTRACTION operation turns up for the applied signal over select line S2 is logical '1', S1 is logical '0', S0 is logical '0'. For the Logical EX-OR operation in Fig. 11 (d) the select line S2 is to be fed with logical '1', S1 logical '0' and S0 logical '1'. The Logical EX-NOR operation is accomplished when the select line S2 is fed with logical '1', S1 with logical '1' and S0 with a logical '0' as shown in Fig. 11 (c). Also, Fig. 11 (e) shows the ADDITION operation is carried out for S2 is fed with logical '1', S1 with logical '1' and S0 with logical '1'.

The simulated output of 8-Bit ALU as shown in Fig. 12 is obtained by simulating the circuit shown in Fig. 6. The voltage applied to the proposed circuit is 0.6 V. The same selection input is applied to all the 1-Bit cascaded ALU's along with the supply voltage. For the different inputs over the selection line, the proposed circuit performs eight different operations, including four arithmetic and four logical operations.

Table 5 shows the obtained results by simulating the 8-bit ALU using FinFET in the cadence virtuoso tool. The 8-bit ALU is designed using Full adder and multiplexers. The key metrics of power, delay, PDP as well as EDP are analyzed for multiplexers, Full adder, 1-bit ALU and for 8-bit ALU.

The results show that the power consumed for the Full adder is 3.6nW, GDI based 2×1 MUX, and GDI based 4×1 MUX is 9.9nW and 19nW, respectively. For the 1-bit ALU it is 26.8nW and 8-bit ALU it is 0.2μW. The delay metrics calculated for Full adder is 4.4ps, GDI based 2×1 MUX, and GDI based 4×1 MUX is 1.3ps and 8.1ns, respectively. For the 1-bit ALU and 8-bit ALU, the delay metrics are 2.17ns and 1.97ns. The product of power and delay is the standard performance parameter which is taken into consideration when comparing standard circuits. The PDP for Full adder is 15.84nW*ps, GDI based 2×1 MUX is 12.87nW*ps and GDI based 4×1153.9nW*ns, 1-bit ALU and 8-bit ALU are 58.15nW*ns and 0.394μW*ns, respectively. The product of energy and delay is also another significant factor which is to be measured. The energy-delay product for Full adder is 69.6J* nW*ps, GDI based 2×1 MUX is 16.731J* nW*ps, and GDI based 4×1is 1246.59J* nW*ns, 1-bit ALU and 8-bit ALU are 126.198J* nW*ns and 0.776J* μW*ns, respectively.

Conclusion

In this paper, the 8 bit ALU is designed using GDI based 4×1 & 2×1 multiplexers and a Full adder. As CMOS has some operational problems like short channel effects which include Drain-induced barrier lowering, high sub-threshold conduction, increased gate oxide leakage,

increased junction leakage, lower output resistance. To overcome the above problems, CMOS is replaced with FinFET. ALU represents the fundamental building block of the central processing unit of a computer, and modern CPUs contains mighty and complex ALU. It performs arithmetic operations, which includes addition, subtraction, increment, decrement, and logical operations, which includes OR, AND, XOR and XNOR. The required gates for these operations are designed using FinFET, and a multiplexer performs logical operations. Here, the power consumption, circuit's delay, in addition to their PDP along with EDP are analyzed which gave the quite better values in terms of power and delay when compared to CMOS technology. The delay of 8-bit ALU is minimized to 1.97ns from 6.95ns and the power consumption reduced to 0.2µwatts from 32µwatts when compared to that of CMOS technology. The FinFET based circuit gave the required output by reducing the delay, power consumption at ultra-low supply voltages.

References

[1] Shiva Taghipour, and Rahebeh Niaraki Asli, "Aging comparative analysis of high-performance FinFET and CMOS flip-flops," Microelectronics Reliability, vol. 69, iss. 2, 2013, pp. 52–59.

[2] S. Swathi, S. Sushma, V. Bindusree, L Babitha, Sukesh Goud. K, S. Chinavenkateswarlu, V. Vijay, Rajeev Ratna Vallabhuni, "Implementation of An Energy-Efficient Binary Square Rooter Using Reversible Logic By Applying The Non-Restoring Algorithm," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[3] Kiran, K. Uday, Gowtham Mamidisetti, Chandra shaker Pittala, V. Vijay, and Rajeev Ratna Vallabhuni, "A PCCN-Based Centered Deep Learning Process for Segmentation of Spine and Heart: Image Deep Learning," In Handbook of Research on Technologies and Systems for E-Collaboration During Global Crises, pp. 15-26. IGI Global, 2022.

[4] Vallabhuni Vijay, V.R. Seshagiri Rao, Kancharapu Chaitanya, S. China Venkateshwarlu, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "High-Performance IIR Filter Implementation Using FPGA," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[5] Jujavarapu Sravana, S.K. Hima Bindhu, K. Sharvani, P. Sai Preethi, Saptarshi Sanyal, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Implementation of Spurious Power Suppression based Radix-4 Booth Multiplier using Parallel Prefix Adders," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-6.

[6] Chandra Shaker Pittala, Vallabhuni Vijay, A. Usha Rani, R. Kameshwari, A. Manjula, D.Haritha, Rajeev Ratna Vallabhuni, "Design Structures Using Cell Interaction Based XOR in Quantum Dot Cellular Automata," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[7] Ratna, Vallabhuni Rajeev, and Ramya Mariserla. "Design and Implementation of Low Power 32-bit Comparator." (2021).

[8] Vallabhuni Vijay, Kancharapu Chaitanya, T. Sai Jaideep, D. Radha Krishna Koushik, B. Sai Venumadhav, Rajeev Ratna Vallabhuni, "Design of Optimum Multiplexer In Quantum-Dot Cellular Automata," International Conference on Innovative Computing, Intelligent Communication and Smart Electrical systems (ICSES -2021), Chennai, India, September 24-25, 2021.

[9] S. Sushma, S. Swathi, V. Bindusree, Sri Indrani Kotamraju, A. Ashish Kumar, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "QCA Based Universal Shift Register using 2 to 1 Mux and D flip-flop," IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[10] M. Sreevani, S. Lakshmanachari, B. Manvitha, Y.J.N. Pravalika, T.Praveen,V.Vijay, Rajeev Ratna Vallabhuni, "Design of Carry Select Adder Using Logic Optimization Technique," IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[11] M. Saritha, Chelle Radhika, M. Narendra Reddy, M. lavanya, A. Karthik, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Pipelined Distributive Arithmetic-based FIR Filter Using Carry Save and Ripple Carry Adder," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[12] S. China Venkateshwarlu, Mohammad khadir, V. Vijay, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "Optimized Design of Power Efficient FIR Filter Using Modified Booth Multiplier," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[13] G. Naveen, V.R Seshagiri Rao, Nirmala. N, Pavan kalyan. L, Vallabhuni Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Design of High-Performance Full Adder Using 20nm CNTFET Technology," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[14] Mohammad khadir, S. Shakthi, S. Lakshmanachari, Vallabhuni Vijay, S. China Venkateswarlu, P. Saritha, Rajeev Ratna Vallabhuni, "QCA Based Optimized Arithmetic Models," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[15] P. Ashok Babu, P. Sridhar, and Rajeev Ratna Vallabhuni, "Fake Currency Recognition System Using Edge Detection," 2022 Interdisciplinary Research in Technology and Management (IRTM), Kolkata, India, February 24-26, 2022, pp. 1-5.

[16] Koteshwaramma, K. C., Vallabhuni Vijay, V. Bindusree, Sri Indrani Kotamraju, Yasala Spandhana, B. Vasu D. Reddy,

Ashala S. Charan, Chandra S. Pittala, and Rajeev R. Vallabhuni, "ASIC Implementation of An Effective Reversible R2B Fft for 5G Technology Using Reversible Logic," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 5-13.

[17] Vijay, Vallabhuni, Kancharapu Chaitanya, Chandra Shaker Pittala, S. Susri Susmitha, J. Tanusha, S. China Venkateshwarlu, and Rajeev Ratna Vallabhuni, "Physically Unclonable Functions Using Two-Level Finite State Machine," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 33-41.

[18] Vijay, Vallabhuni, M. Sreevani, E. Mani Rekha, K. Moses, Chandra S. Pittala, KA Sadulla Shaik, C. Koteshwaramma, R. Jashwanth Sai, and Rajeev R. Vallabhuni, "A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 27-32.

[19] Vijay, Vallabhuni, Chandra S. Pittala, A. Usha Rani, Sadulla Shaik, M. V. Saranya, B. Vinod Kumar, RES Praveen Kumar, and Rajeev R. Vallabhuni, "Implementation of Fundamental Modules Using Quantum Dot Cellular Automata," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 12-19.

[20] Gollamandala Udaykiran Bhargava, Vasujadevi Midasala, and Vallabhuni Rajeev Ratna, "FPGA implementation of hybrid recursive reversable box filter-based fast adaptive bilateral filter for image denoising," Microprocessors and Microsystems, vol. 90, 2022, 104520.

[21] Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, Vallabhuni Vijay, Usha Rani Anam, Kancharapu Chaitanya, "Numerical analysis of various plasmonic MIM/MDM slot waveguide structures," International Journal of System Assurance Engineering and Management, 2022.

[22] Chandra Shaker Pittala, Vallabhuni Vijay, B. Naresh Kumar Reddy, "1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications," Silicon, 2022. https://doi.org/10.1007/s12633-022-02016-8.

[23] M. Saritha, M. Lavanya, G. Ajitha, Mulinti Narendra Reddy, P. Annapurna, M. Sreevani, S. Swathi, S. Sushma, Vallabhuni Vijay, "A VLSI design of clock gated technique based ADC lock-in amplifier," International Journal of System Assurance Engineering and Management, 2022, pp. 1-8. https://doi.org/10.1007/s13198-022-01747-6

[24] B. M. S. Rani, Vallabhuni Rajeev Ratna, V. Prasanna Srinivasan, S. Thenmalar, and R. Kanimozhi, "Disease prediction based retinal segmentation using bi-directional ConvLSTMU-Net," Journal of Ambient Intelligence and Humanized Computing, 2021, pp. 1-10. https://doi.org/10.1007/s12652-021-03017-y

[25] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, M. Saritha, M. Lavanya, S. China Venkateswarlu and M. Sreevani, "ECG Performance Validation Using Operational Transconductance Amplifier with Bias Current," International Journal of System Assurance Engineering and Management, vol. 12, iss. 6, 2021, pp. 1173-1179.

[26] S. Swathi, S. Sushma, C. Devi Supraja, V. Bindusree, L. Babitha and Vallabhuni Vijay, "A Hierarchical Image Matting Model for Blood Vessel Segmentation in Retinal Images," International journal of system assurance engineering and management, vol. 13, iss. 3, 2022, pp. 1093-1101.

[27] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Low power based optimal design for FPGA implemented VMFU with equipped SPST technique," National Conference on Emerging Trends in Engineering Application (NCETEA-2011), India, June 18, 2011, pp. 224-227.

[28] Vallabhuni Vijay, and Avireni Srinivasulu, "A Novel Square Wave Generator Using Second Generation Differential Current Conveyor," Arabian Journal for Science and Engineering, vol. 42, iss. 12, 2017, pp. 4983–4990.

[29] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, and Nakka nikhil, "Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology," VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.

[30] Bandi Mary Sowbhagya Rani, Vasumathi Devi Majety, Chandra Shaker Pittala, Vallabhuni Vijay, Kanumalli Satya Sandeep, Siripuri Kiran, "Road Identification Through Efficient Edge Segmentation Based on Morphological Operations," Traitement du Signal, vol. 38, no. 5, Oct. 2021, pp. 1503-1508.

[31] M. Lavanya, Malla Jyothsna Priya, Ponukumatla Janet, Kavuluri Pavan Kalyan, and Vijay Vallabhuni, "Advanced 18nm FinFET Node Based Energy Efficient and High-Speed Data Comparator using SR Latch," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[32] J. Sravana, K.S. Indrani, Sankeerth Mahurkar, M. Pranathi, D. Rakesh Reddy, and Vijay Vallabhuni, "Optimised VLSI Design of Squaring Multiplier using Yavadunam Sutra through Deficiency Bits Reduction," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[33] L. Babitha, U. Somanaidu, CH. Poojitha, K. Niharika, V. Mahesh, and Vallabhuni Vijay, "An Efficient Implementation of Programmable IIR Filter for FPGA," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[34] K. C. Koteswaramma, Ande Shreya, N. Harsha Vardhan, Kantem Tarun, S. China Venkateswarlu, and Vallabhuni Vijay, "ASIC Implementation of division circuit using reversible logic gates applicable in ALUs," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[35] Vallabhuni Vijay, J. Sravana, K.S. Indrani, G. Ajitha, A. Prashanth, K. Nagaraja, K.C. Koteswaramma, C. Radhika, M. Hima Bindu, N. Manjula, "A System for Controlling Positioning According To Movement Of Terminal In Wireless Communication Based On Ai Interface," The Patent Office Journal No. 50/2021, India. Application No. 202141055995 A.

[36] Dr. L.V. Narasimha Prasad, Dr. Vijay Vallabhuni, Dr. S. China Venkateswarlu, Dr. V. Vhandra Jagan Mohan, Ms. P. Sruthilaya, Mr. K. Tarun Kumar, Mr. B. Raju, Mr. P. Ravinder, "Garbage Collector with Smart Segregation and Method

of Segregation Thereof," The Patent Office Journal No. 04/2022, India. Application No. 202141062270 A.

[37] Sravana, J., K. S. Indrani, M. Saranya, P. Sai Kiran, C. Reshma, and Vallabhuni Vijay, "Realısatıon of Performance Optımısed 32-Bıt Vedıc Multıplıer," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 14-21.

[38] V. Vijay, J. Prathiba, S. Niranjan Reddy, V. Raghavendra Rao, "Energy efficient CMOS Full-Adder Designed with TSMC 0.18µm Technology," International Conference on Technology and Management (ICTM-2011), Hyderabad, India, June 8-10, 2011, pp. 356-361.

[39] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Optimal design of VLSI implemented Viterbi decoding," National conference on Recent Advances in Communications & Energy Systems, (RACES-2011), Vadlamudi, India, December 5, 2011, pp. 67-71.