Journal of VLSI circuits and systems, ISSN: 2582-1458 Vol. 4, No. 1, 2022 (pp. 52-59)

RESEARCH ARTICLE WWW.VLSIJOURNAL.COM

Ultra Low Potential Operated Fundamental Arithmetic Module Design for High-Throughput Applications

O.J.M. Smith[1], F. de Mendonça[2], K.N. Kantor[3], A. A. Zaky[4], G.F. Freire[5]

[1-5]Departamento de Engenharia Elétrica, Universidade Federal de Pernambuco - UFPE Recife, Brazil

KEYWORDS:
Delay,
FinFET,
Logic Gates,
Multiplier,
Power..

ARTICLE HISTORY:
Received 18.07.2022
Accepted 24.08.2022
Published 28.09.2022

DOI:
https://doi.org/10.31838/jvcs/04.01.08

Abstract

The multiplier is an electronic circuit used in digital electronics [1], to multiply two binary numbers. The advantages of the multiplier are low power consumption, regularity of layout, less chip area, high speed etc. Multiplier plays an important role in today's digital processing and various applications. Multipliers are the key components in some high speed systems such as FIR filters, microprocessors, ALU and other commercial applications like computers, mobiles, high speed calculators and some general-purpose processors require binary multipliers. Since last few years, the tiny size of MOSFET, that is less than tens of nanometers, created some operational problems such as increased gate-oxide leakage, amplified junction leakage, high sub threshold conduction and reduced output resistance. To overcome the above problems, FinFET has the advantages of an increase in the operating speed, reduced power consumption, reduced static leakage current is used to realize the majority of the applications by replacing MOSFET. By considering the attractive features of the FinFET, a multiplier is designed as an application. Sequential circuits are extensively used in the design of memory elements such as flip flops and register. Registers are used as data storage devices in low power VLSI designs. The design is simulated using Cadence virtuoso with 20nm technology. Comparative performance analysis is carried out in contrast to the other standard circuits by taking the important performance metrics such as delay, power and power delay product (PDP), energy delay product (EDP) metrics into consideration.

Author's e-mail: smith.ojm@cesmac.edu.br, f.de.mend@cesmac.edu.br, kantor.kn@cesmac.edu.br, fg.freire@cesmac.edu.br

How to cite this article: Smith OJM, de Mendonça F, Kantor KN, Zaky AA, Freire GF. Ultra Low Potential Operated Fundamental Arithmetic Module Design for High-Throughput Applications. Journal of Complementary Research, Vol. 4, No. 1, 2022 (pp. 52-59).

Introduction

The multiplier is an electronic circuit used in digital electronics such a computer,[1] to multiply two binary numbers. Compared to addition and subtraction, multiplication is a complex process.[2] Various computer arithmetic techniques can be used to implement a digital multiplier.[3] Most techniques involve computing a set of partial products, and then summing the partial product together. The binary multiplication follows the same process for producing the product results of the two binary numbers. The binary multiplication is easier as it contains only 0's and 1's.[2-16]

The advantages of the multiplier are low power consumption, regularity of layout, less chip area, high speed etc. Multiplier plays an important role in today's digital processing and various applications.[4] The multiplier is also used in commercial applications like computers, mobiles, high speed calculators and some general-purpose processors require binary multipliers.[17-25]

As the technology advances day-by-day power consumption in battery-operated transportable devices creates a serious concern. MOSFET is widely used now days. Below 45nm technology, controlling the channel of the MOSFET becomes difficult.[5] The other drawbacks of MOSFET implementation are that the power consumption

is high; the delay is also high and large amount of current leaks through the body of the circuit. It also creates operational problems such as gate-oxide leakage, amplified junction leakage, high sub threshold conduction and reduced output resistance.[26]

The FinFET has overcome all the drawbacks of the MOSFET to a great extent. The multiplier using FinFET is designed at 20 nm technology which reduces the silicon area. Using the FinFET the power consumption is reduced and the overall delay of the circuit is also reduced. The operational speed of the circuit is also increased compared to the circuit designed using MOSFET. The operational problems faced by using MOSFET are overthrown by replacing MOSFET with FinFET, the output resistance is increased and the leakages caused by MOSFET which includes gate-oxide leakage and the amplified junction leakage are blown-away.[27-34]

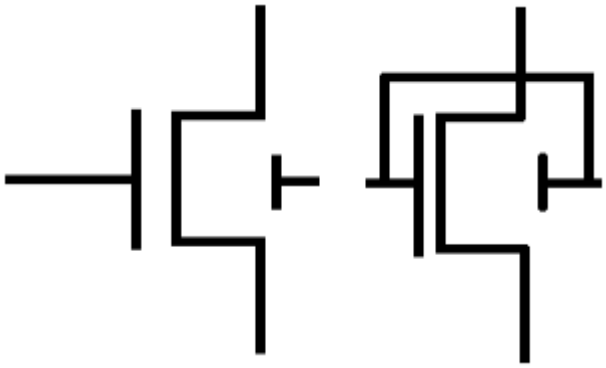
The 2x2 multiplier has two inputs A and B each of 2bit size namely A0, A1 and B0, B1 and it has four outputs Y0, Y1, Y2, and Y3. The circuit designed using MOSFET consists of the following components, they include six AND gates and two EXOR gates. First, the multiplier circuit is implemented using MOSFET in cadence virtuoso tool. The power and the overall delay of the circuit implemented using MOSFET is calculated. The code for the circuit in FinFET using 20nm technology is written, first the program for the individual gates is developed i.e., the code for the AND gate and the EXOR gate are developed, after developing the code for the individual gates then these two programs are combined to develop the code for the entire multiplier circuit and executed using cadence virtuoso tool to get the desired results, the power and the overall delay of the circuit is calculated. Finally results of both the techniques are compared.[35-39]

This manuscript has six sections. The first section is all about the introduction to the existing method, proposed method and the advancements made in the circuit. The second section elaborates the brief information about the FinFET characteristics and modeling. In the third section the entire details of the proposed circuit design and realization of the proposed circuit are discussed. The details about the simulation results of proposed design are presented in the fourth section. Finally, the fifth section consists of the conclusion part of the proposed circuit. The references are attached at the end of the paper.

FinFET Characteristics and Modeling

A Fin Field-effect transistor (FinFET) is a MOSFET built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double gate structure. These devices have been given the generic name "FinFET" because the source/drain region forms fins on the silicon surface. The body of the FinFET is very thin, around 10nm or less. So, there is no leakage path which effectively controls the leakage. The channel is double-gate structure.[7] The drive current of the FinFET can be increased by increasing the width of the channel i.e. by increasing the height of the fin. We can also increase the device drive current by constructing parallel multiple fins connected together. It implies that for a FinFET, the arbitrary channel width is not possible, since it is always a multiple of fin height. So, effective width of the device becomes quantized. While in planner devices, there is the freedom to choose the device's drive strength by varying channel width. It implies that FinFET suffers less from dopant induced variations. Low channel doping also ensures better mobility of the carrier inside the channel.[8]

The basic structure of FinFET is that the conducting channel is wrapped by a thin Silicon fin. This forms the body of the device. The fins are the 3D channel between the source and the drain terminals. They are built on top if silicon (Si) substrate. The gate terminal is wrapped around the channel .The below figure 1 represents the symbolic notation of the FinFET. The "fin" refers to the narrow channel between source and drain. A thin insulating oxide layer on either side of the fin separates it from the gate. FinFET with a thick oxide on top of the fin are called double-gate and those with a thin oxide on top as well as on the sides are called triple-gate FinFET [9]. The figure 2 represents the symbol of the N type FinFET and also P type FinFET.



Fg. 1: Symbolic Notation of FinFET

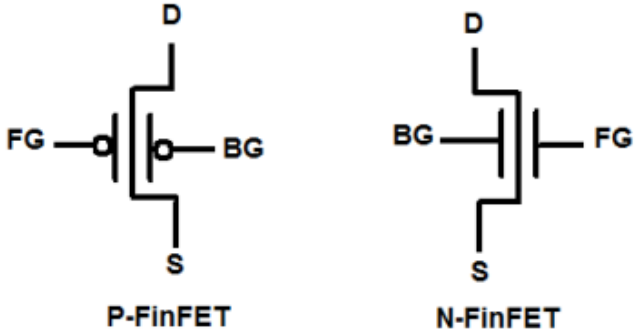


Fig. 2: Symbols of FinFET

The FinFET has better Sub threshold swing than the MOSFET. The control of short channel effect is better in FinFET compared to MOSFET. The FinFET exhibits negligible body effect and also it has very little static leakage. It exhibits high output resistance and high sub threshold conduction.

The advantages of the FinFET are low power consumption, it occupies less chip area and it exhibits high operational speed. It exhibits little or sometimes no body effect and the delay of the circuit is also reduced and the FinFET devices have significantly faster switching times and higher current density than the mainstream MOSFET technology.[10] The FinFET is used only below 45nm technology. It is effectively used to design many combinational and sequential circuits in order to improve their performance characteristics.[11]

Proposed Circuit: Design And Realization

The FinFET has overcome all the drawbacks of the MOSFET to a great extent. The multiplier using FinFET is designed at 20 nm technology which reduces the silicon area. The design is simulated using cadence virtuoso with 20nm technology. Using the FinFET the power consumption is reduced and the overall delay of the circuit is also reduced. The operational speed of the circuit is also increased compared to the circuit designed using MOSFET. The static leakage current is also reduced when compared to that of the MOSFET implementation.

Circuit Diagram

The Fig 3 is the circuit diagram of the 2x2 multiplier. The multiplier has inputs each of 2bits namely a0, a1 and b0, b1 and 4 outputs q0, q1, q2, q3. The multiplier circuit consists of 6 AND gates and 2 EXOR gates.

The Fig 4 represents the circuit diagram of the AND gate. The AND gate is designed using CMOS. The AND gate has inputs namely A and B and output O. In the circuit the NAND gate output is connected to the inverter in order to produce the AND gate output. The AND gate Boolean expression is A.B.

The Fig 5 is the circuit diagram of the EXOR gate. The EXOR gate is designed using CMOS. The EXOR gate has inputs namely A and B and output Y. The EXOR gate Boolean expression is $A \oplus B$.

Truth Table

Truth table of 2x2Multiplier

A0	A1	B0	B1	Y0	Y1	Y2	Y3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Truth table of AND gate

Input A	Input B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

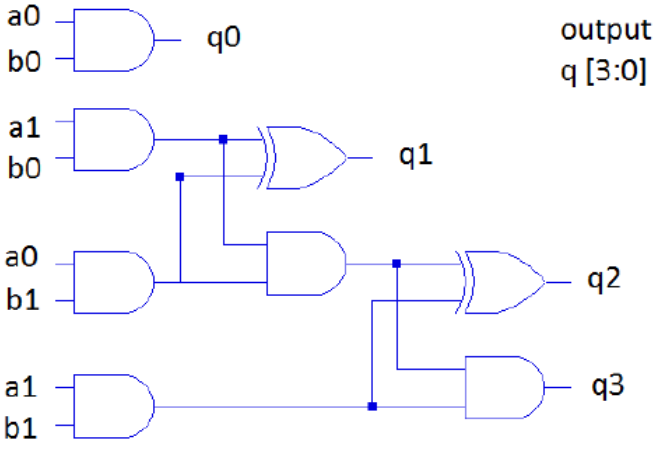


Fig. 3: Circuit diagram of 2x2Multiplier

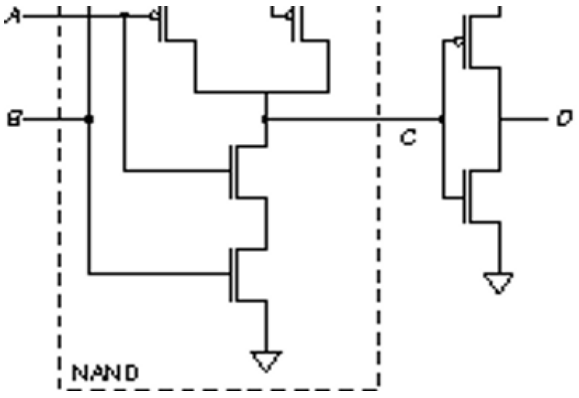


Fig. 4: Circuit diagram of AND gate using CMOS

The basic multiplication algorithm recursively applies the following multiply step to each successive bit of the multiplier beginning with its LSB. AND the multiplier bit with the entire multiplicand, add the result to the accumulating partial product, and shift the accumulating partial product and multiplier one bit to the right. Repeat this step until the MSB of the multiplier has been processed, and read the final product.[12] Consider the multiplication of two 4-bit numbers, as shown in Figure 2. The multiplicand is A1, A0 the multiplier is B1, B0 and the product is y3, y2, y1 and y0. The first partial product is formed by multiplying A1, A0 by B0. The multiplication of two bits such as A0 and B0 produces y0 as 1 if both bits are 1; otherwise it produces 0 as output. This is identical to an AND operation. Therefore, the partial product can be implemented with AND gates as shown in the figure 2. The second partial y1 product is formed by multiplying A0, B1 and is shifted one position to the left. The sum of the two partial products is produced by a binary adder. Note that the least significant bit of the product does not have to go through an adder, since it is completely formed by the output of the first AND gate. The same approach as used for multiplier bit y1 is also used for multiplier bits y2 and y3. Note that the carry out can be 1, so it enters the MSB of the adder at the next level down. In general, for J multiplier bits and K multiplicand bits, we need (J × K) AND gates and (J-1) K-bit adders to produce a product of J+K bits. For the Example multiplier, K=2 and J=2, so we need 4 AND gates and one 2-bit adder to produce a product of 4 bits.[13]

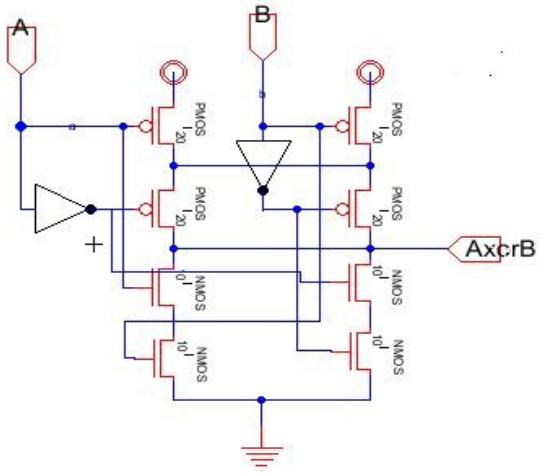


Fig. 5: Circuit diagram of EX-OR gate using CMOS

Truth table of EX-OR gate

Inputs		*Outputs*
X	Y	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Simulation Results of Proposed Method

Transient Response

The Fig 6 is the transient response of the multiplier using MOSFET. In the above graph there are 4 inputs namely net2, net3, net4, net5 and there are 4 outputs namely y0, y1, y2, y3. As the input is varied as shown in the graph corresponding output is produced.

The Fig 7 gives the transient response of the multiplier using FinFET. In the above graph there are 4 inputs namely Va0, Va1, Vb0, Vb1 and 4 outputs namely Q0, Q1, Q2, Q3. As the input is varies with time as shown in the graph corresponding output is produced.

Vdd Vs Delay

The Fig 8 is the graph plotted between Vdd and delay of the multiplier. The output produced by varying the voltage between 0V to 1V is plotted in the above fig 8; the output corresponds to the output of the multiplier realized using FinFET.

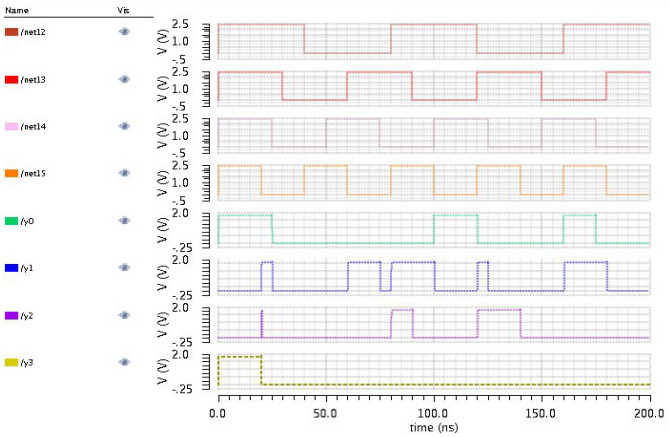


Fig. 6: Transient response of multiplier using MOSFET

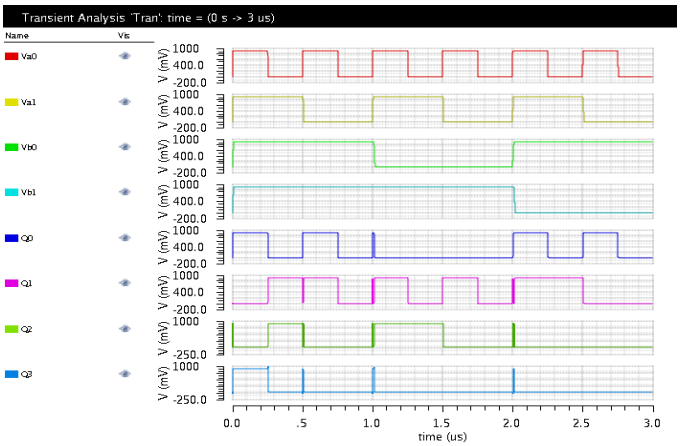


Fig. 7: Transient response of the multiplier using FinFET

Vdd Vs Power

The Fig 9 is the graph which gives the information regarding the power of the multiplier with respect to the voltage variations between 0V to 1V. The graph plotted between Vdd and Power of the multiplier realized using FinFET.

Vdd Vs PDP

The information of the PDP (power delay product) values of the multiplier is plotted in Fig 10. The graph is all about the graph plotted between voltage and the PDP of multiplier realized using FinFET.

Vdd Vs EDP

The Fig 11 is the graph plotted between Vdd Vs EDP (Energy delay product) of the multiplier realized using FinFET. The corresponding EDP (energy delay product) values increases with the increase in the voltage of the multiplier.

Comparative Analysis

The multiplier circuit using FinFET consumes low power and the overall delay of the circuit is minimized to great extent compared to that of the multiplier using MOSFET. Using FinFET very little current is leaked from the body of the circuit. The chip area is minimized and the wafer cost is also cheaper. The operational speed of the circuit is also high.

Multiplier is mainly used in the digital signal processing applications and various applications such as computers and high speed calculators, majorly used in mobiles and general purpose processors, true RMS converter and ring modulator. It is a key component of many high performance systems such as FIR filters, Microprocessors, ALU etc.[14] It is also incorporated into many applications, such as variable-gain amplifier, product detector, frequency mixers. It is effectively used in the companding technique and PAM and automatic gain control.[15]

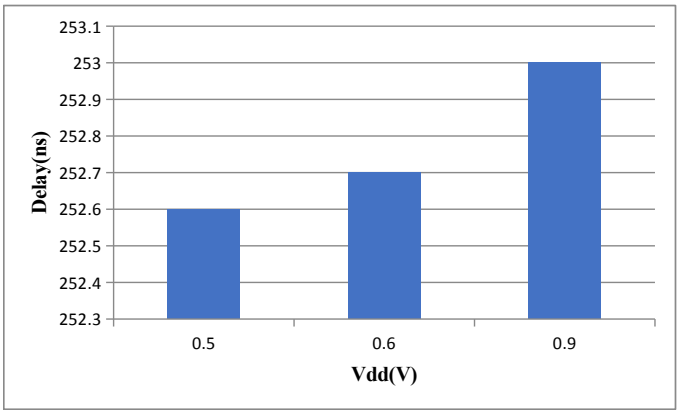


Fig. 8: Graph of Vdd Vs Delay (FinFET)

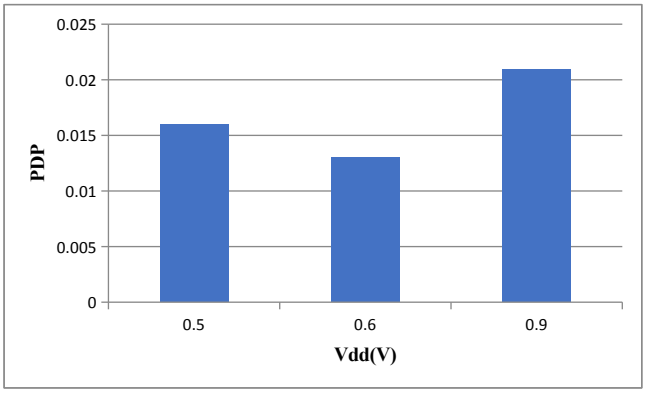


Fig. 10: Graph of Vdd Vs PDP (FinFET).

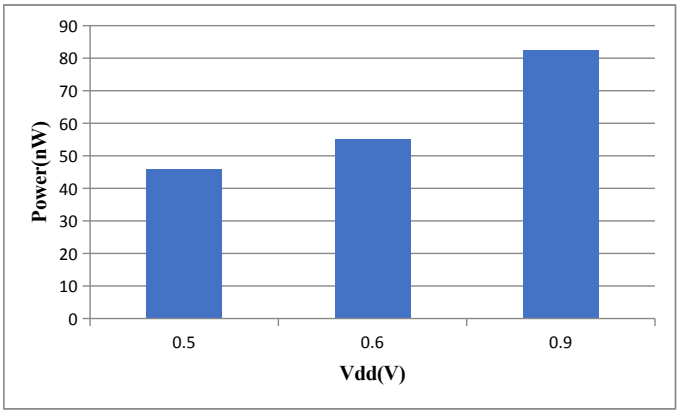


Fig. 9: Graph of Vdd Vs Power (FinFET)

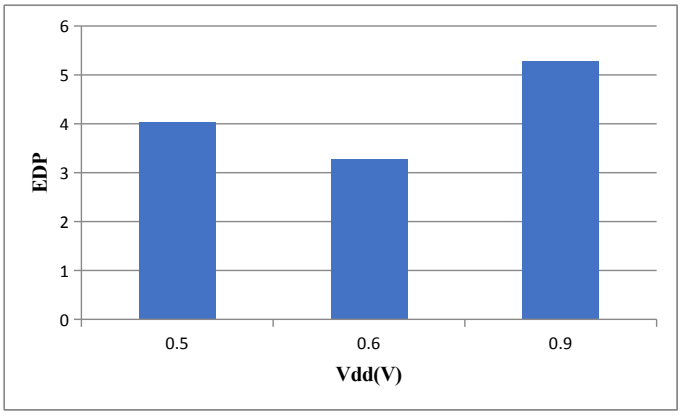


Fig. 11: Graph of Vdd Vs EDP (FinFET).

Vdd(V)	*Power*		*Delay*		*PDP*		*EDP*	
	LVt	*Normal*	*LVt*	*Normal*	*LVt*	*Normal*	*LVt*	*Normal*
0.1	1.74 kW	2.077 uW	7.03 us	16.81 ns	12.23 k	0.03 p	85.97 k	0.000504 a
0.5	41.57 mW	2.497 uW	5.86 ns	3.751 ns	24.36 n	0.009 p	0.0142 f	0.000036 a
0.6	49.89 mW	2.998 uW	5.799ns	3.506 ns	28.93 n	0.0105 p	0.0167 f	0.000033 a

Conclusion

This project implements the optimized low power and high speed FinFET based Multiplier using 20nm technology which is simulated using cadence virtuoso tool. Power performance is improved and delay is improved to great extent. Here comparative analysis of MOSFET and FinFET based Multiplier is also done which shows that FinFET based multiplier at 20nm technology is better than MOSFET based multiplier in terms of power, delay, power delay product(PDP) and energy delay product(EDP). The proposed circuit has some limitations that is the proposed multiplier circuit does not respond for the voltages as given they are 0.2V, 0.3V, 0.4V, 0.6V, 0.7V, 0.9V and 1V. The circuit also limitations like the proposed circuit does not respond for the HVt (high threshold) voltages between 0.1V to 1V.

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