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Research Article

DESIGN OF THE HIGH SPEED AND RELIABLE SOURCE COUPLED LOGIC MULTIPLEXER

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ABSTRACT
As the rapid growth of the VLSI technology over the years the momentum shifts towards the low power and high speed portable electronic devices respectively. Power consumption is one critical aspect which may leads to decreases the reliability and performance of the portable devices. the main aim of this work is to design a low power and high speed Source Coupled Logic (SCL) multiplexer and its analytical model. This circuits can be widely used in mixed signal circuits and high resolution optical fiber links.the proposed circuit was implemented in CMOS 45 nm technology using cadence virtuoso by using industrial technology libraries. And we compared its performances with the existed configurations of the multiplexers with different technology nodes.

Keywords: source coupled logic(SCL),high speed electronic devices.

INTRODUCTION
Multiplexer is one of the most fundamental digital block and which selects the single output among the group data inputs. usually a MUX having 2Nnumber of inputs and N number of the selection lines respectively. The conventional 2 by 1 multiplexer as shown in figure 1 it has two inputs and one selection line. whenever the selection line is zero (S=0) ,its output is A else output is B. The truth table for the 2*1 MUX shown in table 1.

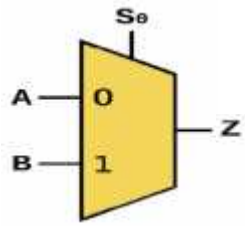

Figure1:Schematic for 2*1 MUX.

Selection Line	Input	Output
0	A(1)	1
1	B(1)	1

Table 1:Truth table for 2 by 1 MUX

The design of the any digital circuits can be done in two configurations such as static CMOS implantation and other one is dynamic CMOS. The static CMOS can be done in by connecting the PMOS transistors in pull up network and NMOS transistors in pull down network respectively[1-4]. By using this configuration model we can get the output swing for any circuit , maintains the good noise margin, low delay and high power consumption. The configuration of the static CMOS shown in figure 2 respectively.

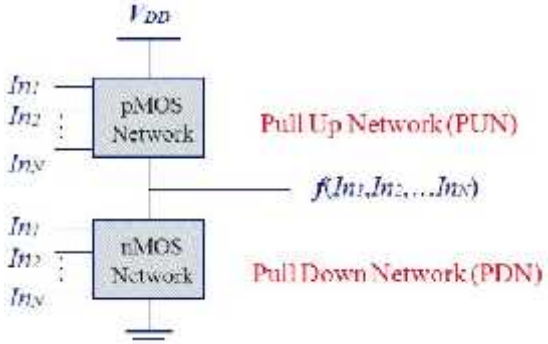

Figure 2: Schematic static CMOS.

On the other hand the same circuit can be implemented using the dynamic CMOS. In order to reduce the total number of the transistors there by increasers the chip density.this set of configuration mainly designed for the sequential circuits[5-7]. The basic configuration for dynamic CMOS as shown in figure 3. and its operation can be done in two ways, such as precharge phase and evaluation phase respectively.

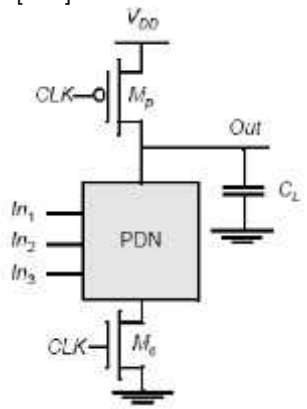

Figure 3: Schematic Dynamic CMOS.

Precharge phase: The operation is mainly depends on the clock signal the output node is precharge up to VDD, during this mode NMOS transistors are in off mode. Hence the path is disabled for the pull down network.

Evaluation phase: When the clock is active high then the prechargetransistor are kept off and evaluation transistor are in turn on mode.Over the past decade VLSI technology provides a great platform for design the high speed ,reliable,reduced area are wide advantageous for the CMOS VLSI.mainly this work emphasise the analysis of different types of CMOS multiplexers[7-10]. The rest of the paper is organised as follows section 2 describes the different types of CMOS multiplexers and section 3 describes the proposed SCL gate based multiplexer and its performance respectively. and final section describes the conclusion.

Existed Literature Survey On Different Types Of Multiplexers

Static CMOS MUX

The static CMOS based 2:1 MUX is designed using the pull-up and pull down network. It consists of four pull up PMOS and pull down network consists of four NMOS transistors. The architecture of the static CMOS 2 by 1 MUX as shown in figure 4.it s final output is fed to the inverter to obtain the accurate output respectively. the input to the MUX can be provide by using the V Pulse.

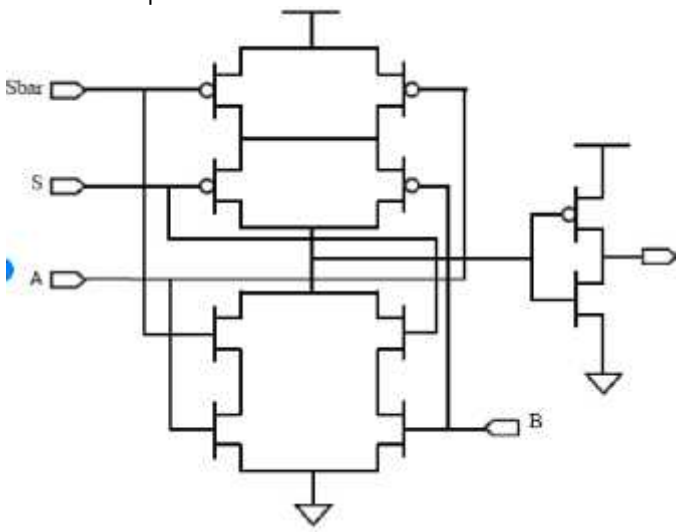

Figure 4: Static CMOS multiplexer.

Domino logic

The design of the domino 2:1 MUX is exactly similar to the Pseudo NMOS logic. The only differences is that the grounded resistor has the higher clock skew. In order to avoid the monotonocity problem and to improve circuit performance using the domino basic logic circuit. Eventually the VDD is connected to the PULL UP circuit and rest of the input are connected to the V Pulse respectively[11].

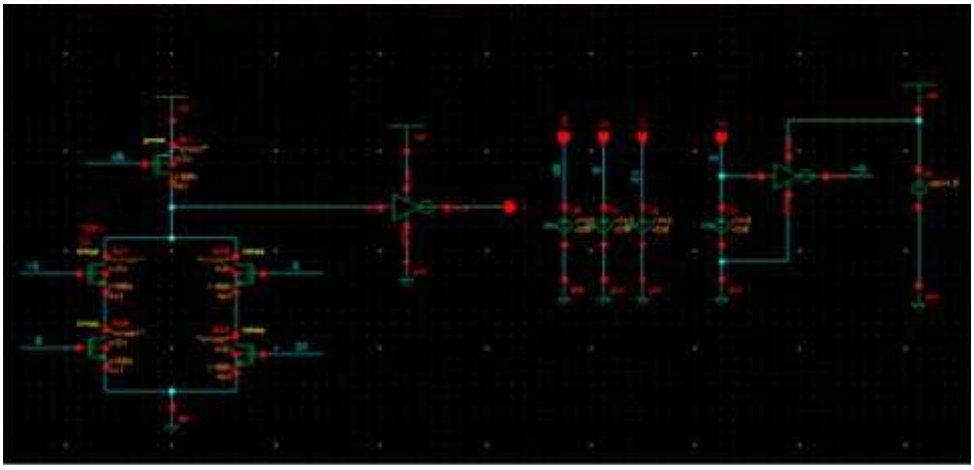

Figure 5: Domino CMOS multiplexer.

Dual rail domino logic

The dual rail domino logic based circuit as shown in figure 6.the operation and working principle are similar to the domino logic[12].

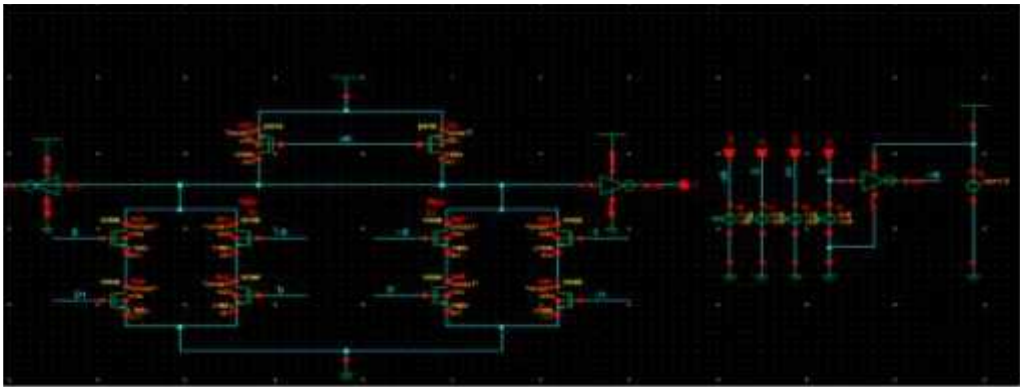

Figure 6: Domino CMOS multiplexer.

Comparison of different types of Multiplexers

The table 2 clearly describes the different types multiplexers whose performance metrics such as no of transistors required to design the architecture, amount of average power, total delay, power delay product and area respectively.

Table 2: Performance indication of different logic styles of transistors

Name of the logic	No of transistors	Average power(W)	Delay (s)	Power Delay Produce (PDP) (J)	Area (m)
Static CMOS	12	55.33µ	4.573n	0.253	4.32p
Pseudo NMOS	7	411.5µ	4.561n	1.87	2.52p
Domino logic	**7**	**126.2µ**	**4.5505n**	**0.574**	**2.52p**
Dual Rail domino	14	248.8µ	4.5515n	1.13	5.04p

Proposed Scl Mux

Source Coupled Logic (SCL) based multiplexer consisting of the four NMOS transistors and two PMOS transistors. It is it acts like a switch when it operated in saturation region. the bias current $I_B$is two output branches by source coupled pairs. In order to garmented the performance the output of the each current path will be transferred to same direction. The circuit diagram of the SCL based multiplexer and whose layout as shown in figure 7 and 8 respectively.

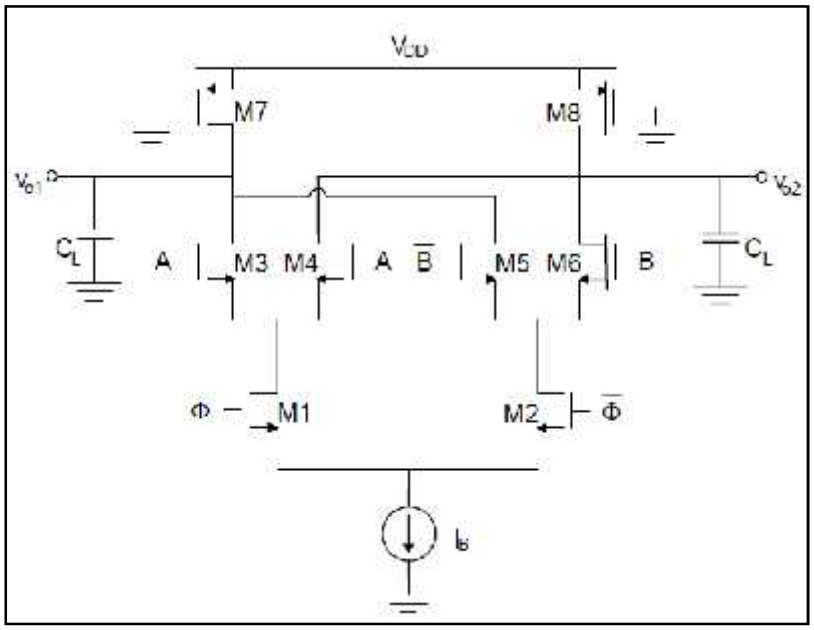

Figure 7: SCL based multiplexer

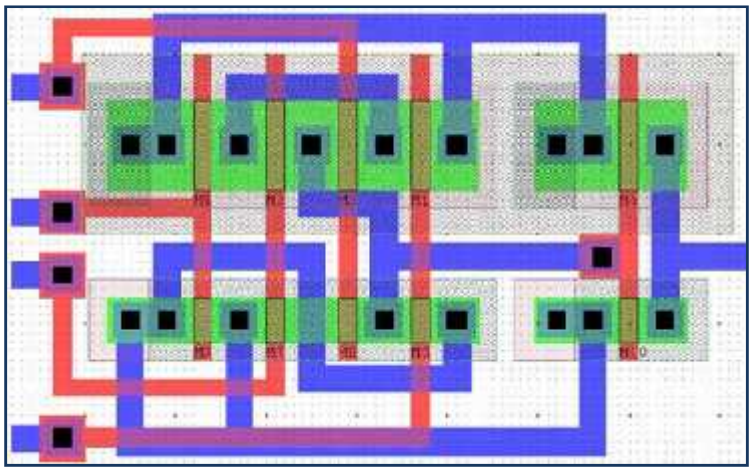

Figure 8: Layout of the SCL based multiplexer.

Conclusion

This paper is aims to study the performance of the different types of the multiplexers and its parameters such as delay, noise margin, powerdissipation, energy delay product respectively. The proposed circuit can be easily implemented in any portable devices like FPGA/CPLD design.

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