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1.8-V Low Power, High-Resolution, High-Speed Comparator With Low Offset Voltage Implemented in 45nm CMOS Technology

Ishrat Z. Mukti[1], Ebadur R. Khan[2]. Koushik K. Biswas[3]

1-3Dept. of EEE, Independent University, Bangladesh, Dhaka, Bangladesh

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Abstract

This paper presents the design of a comparator with low power, low offset voltage, high resolution, and rapid speed. The designed comparator is built on 45 nm flip CMOS technology and runs 4.2 G samples per second at nominal voltage. It is a custom-made comparator for a highly linear 4-bit Flash A/D Converter (ADC). The outlined design can operate on a nominal supply of 1.8 V. The comparator offset voltage was elevated because of this mismatch. To compensate for the offset voltage, we followed a decent approach to design the circuits. Therefore, the offset voltage is reduced to 250μV. The designed comparator has a unity gain bandwidth of 4.2 GHz and a gain of 72dB at nominal PVT, which gives us a considerable measure of authority. The dynamic power consumption of the comparator is 48.7μW. The layout of this designed comparator has been implemented, and the area of the comparator is 12.3 μm × 15.75 μm. The results of pre-and post-layout simulations in various process, voltage, and temperature corners are shown.

Author's e-mail: ishratzahanmukti16@gmail.com, **ebad.eee.cuet@gmail.com, koushikkumarbiswas13@gmail.com**

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Introduction

A comparator is a device that compares between two input signals, basically an input analog signal with a reference signal, and gives outputs in terms of a digital signal based on the result of the comparison. Comparators are widely used in various circuits, especially A/D converters (ADC). An ADC application is one that requires a quicker operating speed and reduced power consumption. They also aim for a reduced noise level and a lower offset voltage. The comparator is crucial in obtaining greater operating speeds and lower power consumption. The comparator we suggest is made using CMOS technology, which has strong noise immunity and low static power consumption. This article details the design of a comparator for use in a 4-BIT FLASH ADC with a sampling rate of 4.2 GHz. In such a circumstance, the device's accuracy should be no less than 1/2 LSB. When the reference voltage and supply voltage are identical, the LSB value of an N-bit ADC is provided by the following formula:

$$LSB = \{VDD/ (2) \hat{} N\} \quad (1)$$

The desired comparator resolution is 112.5 mV for a 4-BIT converter with a 1.8V supply voltage. In this work, we examine the design and operation of a current-based, low-power comparator. In order to gain more precision and minimize, a competent offset cancellation method has been implemented. In this comparator, super low threshold MOSFETs are used. In general, in a conventional MOSFET structure, the gate capacitance tends to show a higher value. For this reason, the threshold of the MOSFETs tends to be higher. One of the techniques to obtain a super low threshold of MOSFETs is to fabricate the MOSFETs with lower gate capacitance. As the gate capacitance is lower in these types of MOSFETs, the threshold voltage will reduce a lot which will give a better headroom for design, to have a great ICMR range, low power consumption, and large obtainable gain while keeping all the MOSFETs in saturation. SLVT MOSFETs allow doing that. Also, the length

of the MOSFETs was increased to four times of the nominal length which has provided the design with a better Noise Figure, PSRR, Gain, and CMRR performance.

Related Work

Over decades, the design of a comparator has been implemented. With the use of various process technology, several researchers have produced a variety of acceptable comparator structures for a variety of applications.

Developed a three-stage voltage comparator concentrated on improving comparator sensitivity and total gain in this design. B. Prathibha et al.[2] suggested a three-stage CMOS comparator with a high-speed operation to gain a lower static & dynamic power dissipation and a smaller offset voltage. Satyabrata et al.[3] compare the traditional comparator to the latched and hysteresis-based comparator. Zbigniew[4] presented the design of a comparator for a high-linearity flash ADC, which was realized in a 22nm FDSOI process with a 0.8V supply. The architecture of a pipelined ADC mismatch insensitive dynamic comparator.[5] High-resolution comparators have also been designed utilizing offset measurement and a cancellation technique involving dynamic latches.[6] Consequently, it was suggested to build a dynamic comparator with high accuracy and low offset.

This paper focused on the highly linear, low offset voltage, high resolution, and low power performance of the Comparator. The comparator design given in this paper is designed that can be used with flash ADC.

Architecture of Comparator

The comparator circuit is the essential element of every ADC. The total performance of the ADC is determined by the properties and performance of the comparator. Fig. 1 depicts the block diagram of the proposed comparator. This topology comprises two blocks in it.

- OTA Stage
- Output Stage

Up to the OTA, the stage amplification of analog input is performed. Then the buffer stage further amplifies to give a level as well as strengthen the OTA OUTPUT signal for load driving. After the output buffer stage, a digital signal is created on the output side. Fig. 2 depicts the schematic of the entire idea.

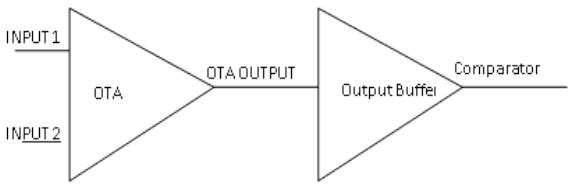

Fig. 1: Block diagram of the suggested Comparator

A. Operational Transconductance Amplifier

OTA is a fundamental component in the majority of analog circuits with linear input-output characteristics. It is essentially identical to conventional operational amplifiers in which differential inputs are present. The primary distinction between OTA and traditional OPAMP is that the output of OTA is in the form of current, while the output of conventional OPAMP is in the form of voltage. The comparator has two special properties.

- Input Swing
- Output Swing

Our target is a small change of ΔVGS as if we get a sharp digital output in the comparator. We know, Inverter has a very high gain. We make the OTA stage by connecting a differential amplifier with an Inverter. All the MOSFETs

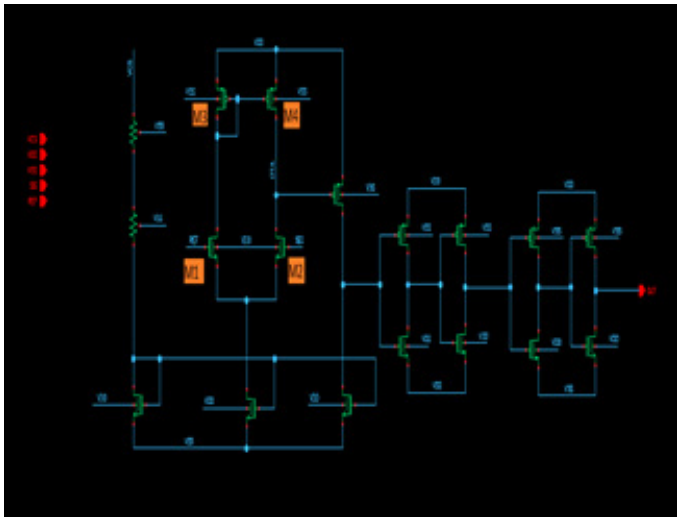

Fig. 2: Schematic of the 45nm CMOS-based Comparator

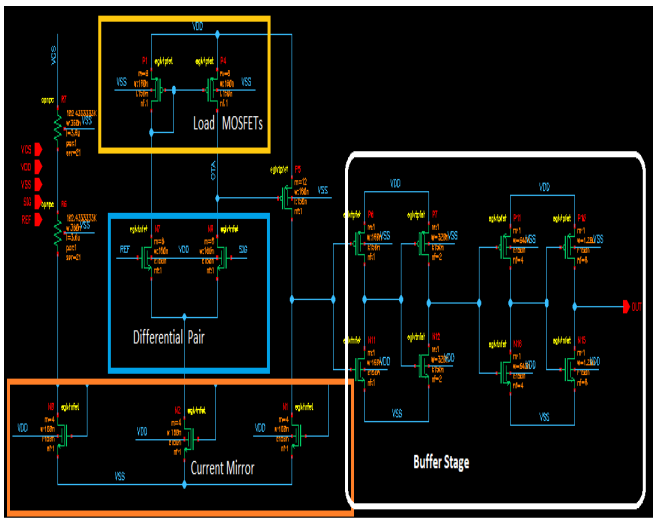

Fig. 3: Differential Pair, OTA Stage, and Current Mirror for The Comparator

of the OTA stage are in saturation. Transistor size is very important. It affects a lot of performance, and a lot of parameters. By making the Differential Amplifier Circuit, we have only four MOSFETs for the differential section, one MOSFET for reference current, and one MOSFET for current mirror Fig. 3 If there is no difference between inverting to the non-inverting terminal, then the internal circuit remains balanced. For simplification, we change the width of the MOSFETs. If we change the length of the MOSFETs then the channel length modulation will be hard to control as well as the matching properties. In Fig. 2, M3 and M4 are independent of M1 and M2 but they are depending upon each other. When the circuit is in a balanced condition in differential pair we will find an equal amount of current. we can minimize the size of the MOSFETs in this way. Differential voltage gain is much higher than single-ended voltage gains.

We want to amplify the output in a high-impedance node in the OTA stage. When we take the output voltage from the MOSFETs drain terminal, the output voltage will be inverted. To make a high-impedance node, we have one NMOS and one PMOS. NMOS is used as a current mirror. The NMOS drain terminal and PMOS drain terminal are connected to each other Fig. 3, which is a basic configuration of an inverter. If the voltage is slightly changed, the output will become high to low or vice versa. To minimize the output offset voltage, we use the Inverter beta ratio Fig. 4.

A. Output Stage

It's the last step of the design process that serves as a buffer. The buffer circuit prevents the source from becoming overloaded. Because of the low value of the load, the voltage source is essentially shortened and draws too much current from the source, which is detrimental to the source. For example, cascading a buffer after a source allows for the division of labor—the source only generates a correct voltage and the corresponding current, and because of the high impedance of a buffer's output, it draws no current from the source and therefore prevents loading.

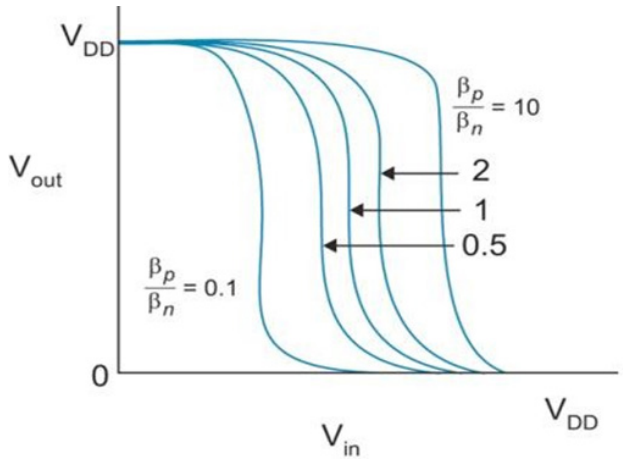

Fig. 4: Beta ratio of Inverter

Comparator Performance

The design of this Comparator is done using Cadence Tool. The Simulation results are done using Cadence Spectre environment using 45nm CMOS technology. The simulation result of the comparator shows that the OPEN LOOP GAIN of approximately 72dB. The Comparator has UGBW of about 4.2 GHz in the nominal corner. Table 1. shows the design and performance parameters on different PVT corners of the Comparator. The AC response which shows gain and phase change with frequency is shown in Fig. 5. The Transient response with input in the pulse is depicted in Fig. 6.

Table 1: Design and Performance Parameter on Different Pvt Corner

Specification	Simulated			Unit
	Typical	Fast	Slow	
Temperature	25	125	-40	°C
Supply Voltage	1.8	1.98	1.62	V
Gain	72.4	68.49	74.46	dB
Bandwidth	4.241	4.728	3.508	GHz
Current	27.06	42.1	18.685	µA
Power	48.7	83.37	30.27	µW

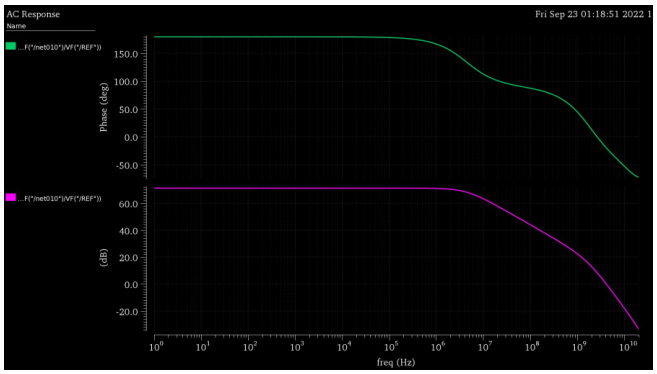

Fig. 5: AC analysis of the Comparator

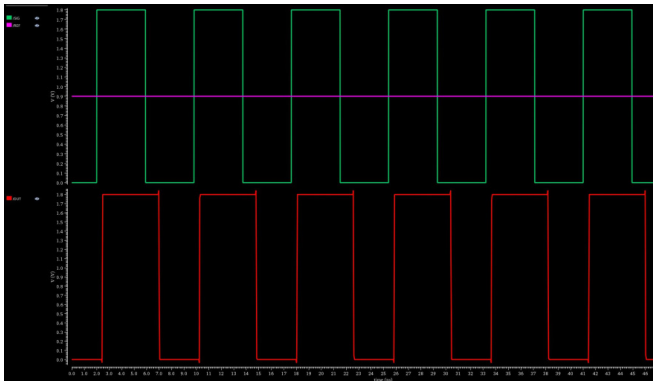

Fig. 6: Transient Analysis of Comparator

The electrical characteristics of different PVT Corners of the Comparator are included in Table 2. By using DC sweep the offset voltages of the comparator are calculated for a range of supply voltages. The supply voltage has ranged between 1.62V and 1.98V, while the input voltages have been set to 0.9V. The offset voltage is found by subtracting the output voltage from 0.9 V. **Fig. 7.** depicts the waveform of the voltage offset. The measured offset voltage is 250μV.

Table 3. shows the Switching Characteristics of the Comparator. Propagation delay is shown in Fig. 8. at Temperature = 25°C, Supply Voltage = 1.8 V, and input overdrive = 100 mV

The outcomes of a Monte Carlo simulation (100 iterations) of the comparator in process variation and mismatch mode can be seen in Fig. 9. Monte Carlo is used to estimate the possible outcomes of an uncertain event.

Fig. 10 depicts the operational amplifier's layout. The PMOS and NMOS are separated at the top and bottom, respectively. They are arranged in such a way as to have the smallest possible area. For a well-matched arrangement, the actual transistors have been sur- rounded by dummy transistors.

Table 2: Electrical characteristics on different pvt corner

Parameter	Electrical characteristics			Unit
	Typical	Fast	Slow	
Temperature	25	125	-40	▫
Input offset Voltage	250	450	46	μV
PSRR	85.1	570	429.11	μV/V
VCM	191.7	472.3	163.3	μV
CMRR	81.2184	80	82.5867	dB
Voltage Output High from Rail	0.0142	2.563	0.0034	mV
Voltage Output Low from Rail	0.002	0.0024	0.0016	mV
Specified Voltage	1.8	1.98	1.62	V
Operating Voltage	1.8	1.98	1.62	V

Fig. 7: DC Analysis for Offset Voltage

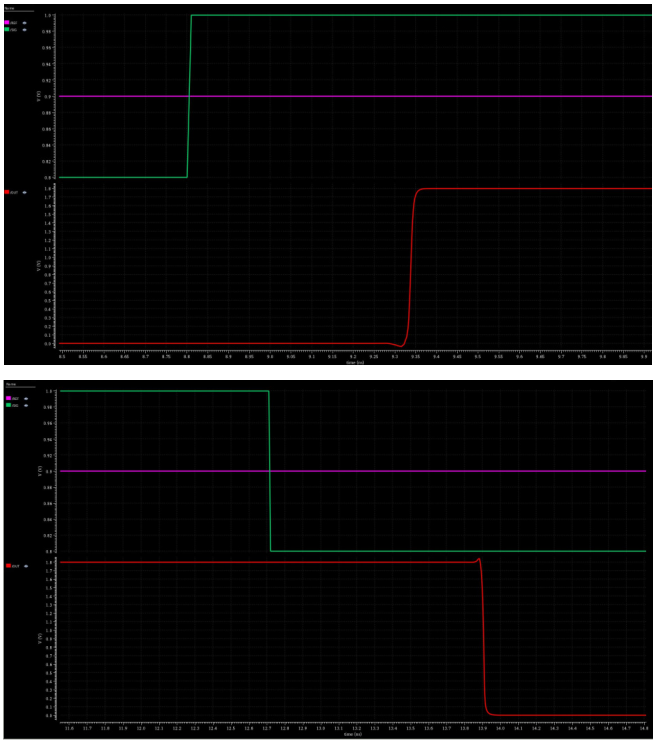

Fig. 8: Propagation Delay

Table 3: Switching characteristics of the comparator

Parameter	Test Condition	Typical(pS)
Propagation Delay Time, Low to High	Input Overdrive 10mV	94.347
	Input Overdrive 100mV	141.058
Propagation Delay Time, High to Low	Input Overdrive 10mV	110.85
	Input Overdrive 100mV	149.35
Rise Delay	500fF	3026.6
Fall Delay	500fF	2239.8

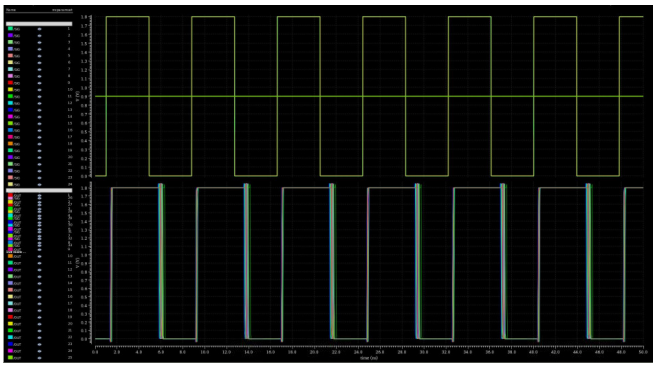

Fig. 10: Monte Carlo Simulation (100 Iterations)

Separating PMOS and NMOS with guard rings. Metal- 1 and Metal-2 are utilized for NMOS and PMOS connectivity. Current source resistance is positioned underneath MOSFETS so that high temperatures do not interfere with the signal. Metal 3 is used for connections at a higher level.

Fig. 11. depicts the post-layout transient analysis response of the comparator at temperature 25¤ and input overdrive voltage 20mV. The output waveform is quite nearer to the pre-layout simulation. Switching characteristics, propagation delay, current, and power all results are given satisfactory results.

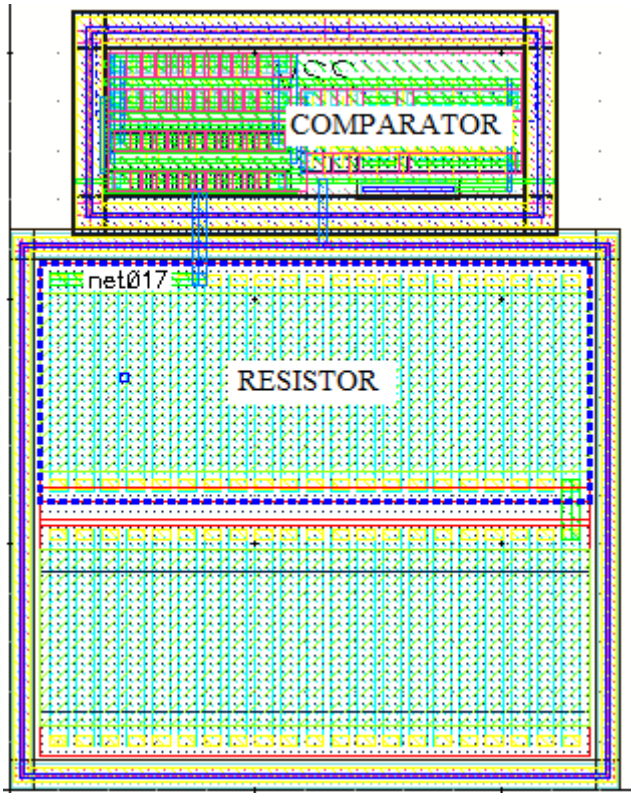

Fig. 10. Layout of Comparator

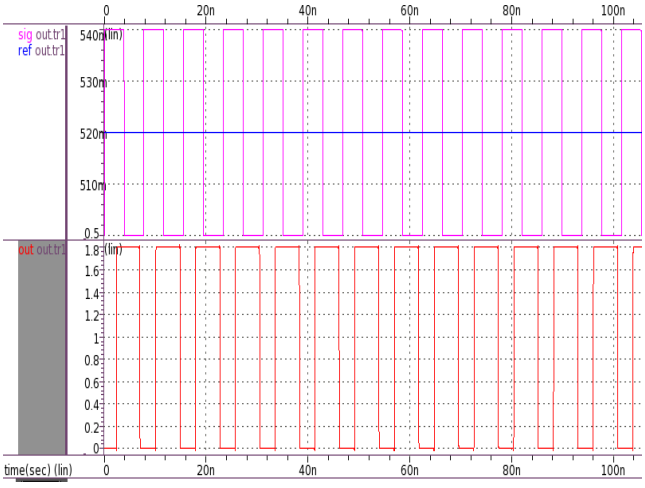

Fig. 11:Post Layout Simulation Result

Table 4: Post layout simulation results

Specification	Simulated Typical	Unit
Temperature	25	¤
Supply Voltage	1.8	V
Rise Delay	40	pS
Fall Delay	46	pS
Current	31.06	µA
Power	56.04	µW
Propagation Delay Time, Low to High	2.32	nS
Propagation Delay Time, High to Low	3.3	nS

The Table 4. Shows the post layout simulation results at Temperature 25¤, Supply voltage 1.8V, Typical corner, Input Voltage 520 mV, and overdrive voltage 20 mV.

Conclusion

This research presents the design of a comparator devoted to high linearity flash ADC. Using 45 nm CMOS technology with a low supply voltage of 1.8V, it has been shown that high-resolution execution is attainable. Transistor mismatch, which results in relatively large offset voltage, is the main obstacle to obtaining high-performance design. Utilizing a single comparator block to compare the input signal to all reference voltage levels is the conventional way of constructing Flash ADCs. This implies that a single Comparator must be tuned to guarantee that all instances of comparators function properly. In this study, the design and testing of a single comparator circuit are presented. The comparator is built and simulated in Cadence using CMOS technology based on 45nm technology. It was shown that the suggested Comparator can run with a 1.8V supply, a 250µV offset voltage, and a low power consumption of 48.7µW at the nominal Corner.

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