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Design and VLSI implementation of SAR Analog to Digital Converter Using AnalogMixed Signal

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Abstract

The creation of an 8-bit SAR ADC with a 0.8V and 5V input voltage is discussed in the publication. Cadence Virtuoso software was used to implement the design, which made use of both 180nm and 90nm technology. The comparator block, which was created using Verilog code and required to operate properly, was the main emphasis of the design. Since the comparator is the block that uses the most power overall, optimising it took up a sizable chunk of the design process. The DAC sub-block was implemented using an MDAC network to increase the ADC's accuracy. The ADC was driven by asynchronous control logic, which was implemented using Verilog code and did not require a clock signal.

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Introduction

Analog data must be transformed into a digital format in order to be effectively used, as digital media has taken over as the primary method for accessing, storing, and disseminating information. However, the analog way in which the digital world finally communicates with the physical world necessitates analog to digital conversion on the receiving end of communication networks. For power-constrained systems, portable and implantable devices, and high-performance computer systems that demand optimisation in terms of power consumption, space usage, and speed, this conversion process is particularly important. Given the significance of analog to digital conversion, communication system designers must give careful consideration to the design of ADCs. Depending on the individual needs of the system, different types of ADCs, such as Flash, Sigma Delta, and SAR ADC, offer a variety of benefits and drawbacks. For instance, Flash ADCs provide an output in a single cycle, which is the fastest conversion time available. However, as the number of bits and resolution rises, the number of comparators needed also sharply rises, necessitating a corresponding rise in power and space utilisation. Sigma Delta ADCs (or integrating ADCs) have the highest resolution but are the slowest and most difficult to construct, so they may be used if higher resolution is the only criterion. ADC selection ultimately depends on the particular requirements and limitations of the system, and optimising ADC design requires careful consideration of these aspects.

To increase conversion speed and reduce power consumption, advanced and hybrid ADC designs such as pipelined Flash, pipeline SAR, and flash SAR have been created and studied. These architectures try to keep the number of components to a minimum while still using power effectively, however there is only so much power consumption can be cut. Due to its outstanding power efficiency, the SAR ADC has stood out among these designsand is now a crucial research topic for applications requiring medium resolution, high speed, low power, and low area. Due to its straightforward design, low power requirements, and flexibility to scale with technology, SAR ADCs have become a popular choice for biomedical applications. This is mostly because, with the exception of the comparator, most of their blocks or components are digital. Numerous studies have been done to enhance the performance of SAR ADCs, with a focus on split capacitor [5], charge recycling [7], and other methods. By analysing and developing the comparator and DAC and using a differential amplifier to reduce distortion and improve common mode noise reduction, this study specifically aimed to reduce power consumption. As a

second level of amplification, a common source amplifier stage was used to make sure the transistor stays in the saturation area.

The section II of the article explains the fundamental structure of SAR ADC. Following that, the section III illustrates various blocks with their schematics that constitute the architecture and explains the functioning of the control logic. The IV and V sections present the simulation outcomes and final remarks, respectively.

SAR ADC ARCHITECTURE

A SAR ADC's block diagram normally has a number of parts. The input analog signal is first sampled by a Sample and Hold (S/H) circuit or Track and Hold circuit. The output of the DAC is compared with the sampled reference signal using a comparator next. The Successive Approximation Register (SAR), which determines each bit consecutively, is the analog counterpart of the output of the control logic and is created by the DAC itself. Finally, the output of the comparator is transformed into its digital equivalent by the SAR control logic using the binary search method. Overall, the SARADC architecture uses a multi-component system that depends on the interaction of the S/H circuit, comparator, DAC, and SAR management logic to reliably and quickly convert analogue signals to digital data.

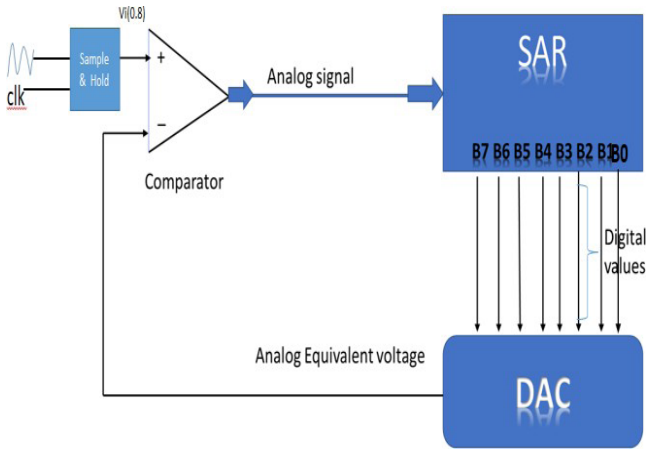

Fig. 1: Block Diagram of SAR ADC

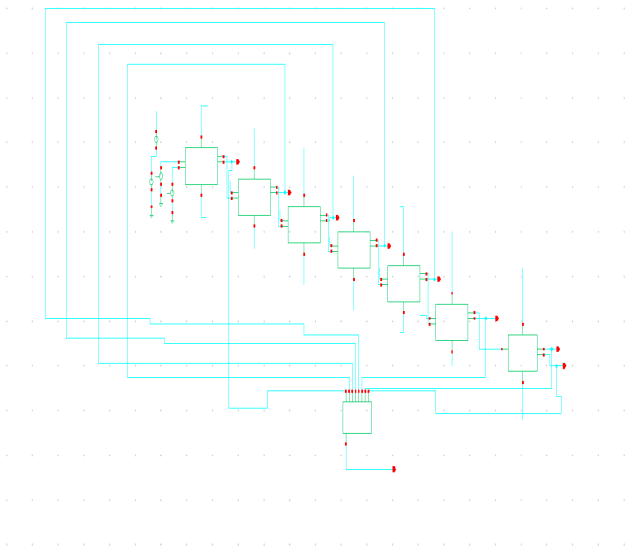

Fig. 2: Schematic Diagram of SAR ADC in CadenceVirtuoso

The SAR ADC implementation diagram using Cadence Virtuoso is shown in Figure 2.

CIRCUIT IMPLEMENTATION

The various components shown in Figure 1 have been realized in Cadence Virtuoso and their details are explained below.

Sample and Hold Circuit (S/H)

A MOS switch and a capacitor are frequently used to create a sample-and-hold (S/H) circuit, with the switch acting as a conduit for the input signal (Vin) to charge the capacitor during the sample mode when the clock at the transistor gate is high. A differential amplifier stage is often employed at the output of the S/H circuit to eliminate any potential loading impact. The MOS switch serves as an open circuit in the hold mode while the clock is off, keeping the capacitor from draining and maintaining the voltage value that was sampled during the arrival of the clock pulse. This indicates that the capacitor maintains the input voltage value throughout the hold mode until the next clock pulse, at which point it charges once more. Either directly across the capacitor or at the differential amplifier's output, the output can be achieved.

Comparator

One of the main sources of power consumption has been identified as the comparator, a crucial part of this system. In order to ensure that the MOS transistors used in its construction work in the saturation area, which is essential for effective amplification, a great deal of effort was put into its design. The differential amplifier was also used to reduce the effect of noise, which can damage the output signal's quality. The primary function of a comparator is to compare the input voltage to the reference voltage and, depending on the comparison's outcome, to generate a logic output that is either high or low. The comparator has better operational speed and great resolution as a result of the thorough design, making it a highly useful part of this architecture.

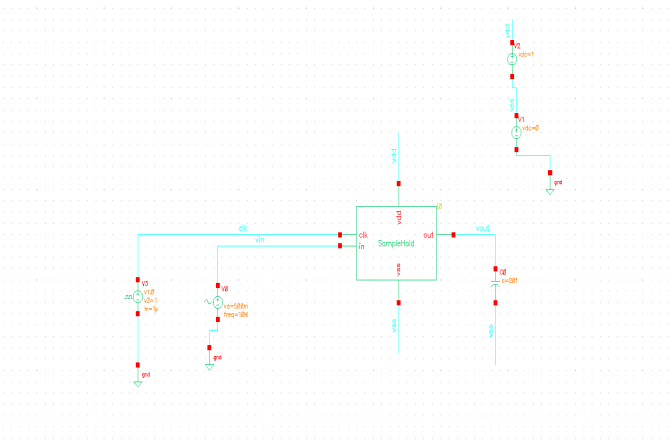

Fig. 3: Schematic Diagram of Sample and Hold Circuit

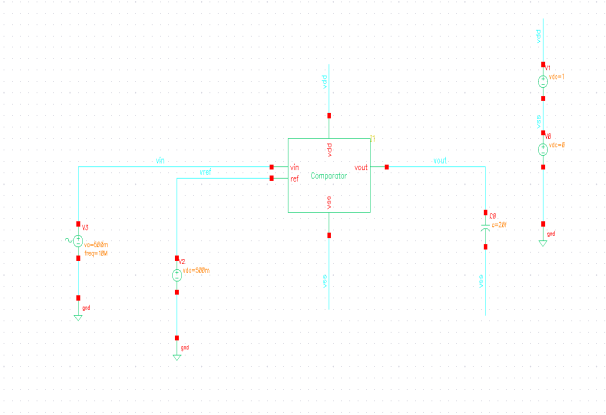

Fig. 4: Schematic Diagram of Comparator

Digital to Analog Converter

Digital-to-analog converters (DACs) can be implemented in a variety of ways, each with advantages and disadvantages of its own. The binary weighted resistor array, one of the most popular DAC designs, creates the correct output voltage using resistors of various values. However, this method is unsuitable for high-resolution DACs since the area needed to fit the extra resistors grows as the number of bits increases. Additionally, as the number of bits rises, the matching of resistor values gets more difficult and might result in inaccuracies in the output voltage.

The weighted capacitor approach is another way to design a DAC, but it also has the drawback of having area requirements that rise with the amount of bits. However, compared to the binary weighted resistor array, this method typically uses less space. Despite this benefit, it still struggles to produce accurate voltage outputs since capacitor values must be precisely matched.

The split capacitor array is a different way to design a DAC that uses less space and power than both the binary weighted resistor array and the weighted capacitor technique. Split capacitor technology, on theother hand, boosts parasitic capacitance, which can contribute more noise and distortion to the output signal. All things considered, the unique application requirements and trade-offs between accuracy, area, and power consumption will determine the DAC implementation method to be used.

To enhance accuracy, the Multiplying DAC network was utilized in the implementation of theDAC block.

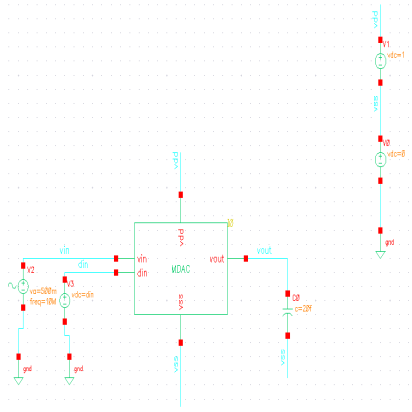

Fig. 5 Schematic Diagram of Multiplying DAC

Successive Approximation Register Logic

The Successive Approximation Register (SAR) control logic is a crucial component in Analog-to- Digital Converters (ADCs) that enables the determination of each bit successively. Essentially, the SAR register consists of N flip flops for an N-bit ADC, as well as some combinational logic, and it implements the binary search algorithm for its operation. During the ADC conversion cycle, the SAR performs a binary search through all possible bits, with each bit having three possibilities: it can be set to '1', reset to '0', or maintain its value. At the start of the conversion cycle, the SAR is reset by holding a start signal high, and on the positive edge of the first clock pulse, the Most Significant Bit (MSB) is set to '1', while the other bits are reset to '0'. The Digital-to-Analog Converter (DAC) then generates an analog equivalent of this digital word, which is then compared with the sampled analoginput signal by the comparator. If the DAC output is lower than the sampled input, the comparator gives a LOW output, and the SAR MSB will be reset to '0'. Conversely, if the DAC output is higher than the sampled input, the comparator gives a HIGH output, and the SAR MSB will be retained, and on the positive edge of the next clock pulse, the next MSB will be set to '1'.

This process is then repeated for the other bits until each bit of the SAR is determined. As soon as the Least Significant Bit (LSB) is tried, the SAR forces the conversion complete signal HIGH to enable the latch to give the valid data in digital form. It should be noted that in this case, "N+1" clock cycles are required for an N-bit ADC. There are two primary approaches to designing the SAR logic: the first involves a ring counter and a shift register, which requires 2N flip flops, while the second approach requires N flip flops and some combinational logic, which was used in this paper.

SIMULATION RESULTS

Using 90nm and 180nm technology, the work detailed in the report has been carried out in Cadence Virtuoso. Different independent analyses, including transient, AC, and DC analyses, were carried out for various sub-blocks. The calculator option was used to calculate how much power each block used. The waveforms produced by the simulation are displayed in the following figures.

The Fig. 6 shows the transient response of Sample and Hold circuit that applies an input analogue signal (Vin) to the source terminal of the MOS switch, which is coupled to a clock signal (Vclk) that controls the MOS switch's on/off state. The switch samples Vin and samples the output signal (Vs) depending on the state of the clock or control signal. The S/H block uses very no energy. Plotted in Fig. 7 is the comparator's response (circuit schematic shown in Fig. 4). The input signal (Vin) is applied to the comparator's other terminal (the inverting terminal) while one terminal is grounded. The comparator compares the two inputs and produces an output that is amplified as a result. The output will enter a negative cycle and vice versa if the input of the inverting terminal is higher than the input of the non-inverting terminal.

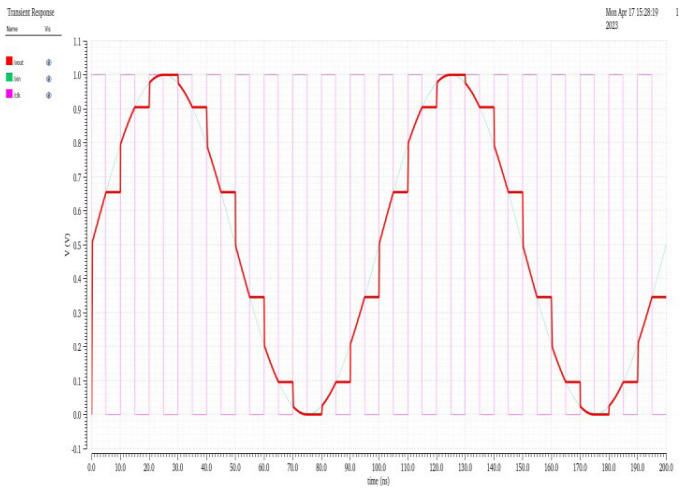

Fig. 6: Transient Response of Sample and Hold Circuit

The conversion cycle begins with a reset of the Fig. 8 and 9, 8-bit data acquired from the output of SAR control logic (Fig. 1) is sent into the DAC circuit in Fig. 5, which generates an analogue signal as its output. For the 90nm technology, this procedure moves at a rate of 50Msa/s, and for the 180nm technology, it moves at a rate of 1Gsa/s.

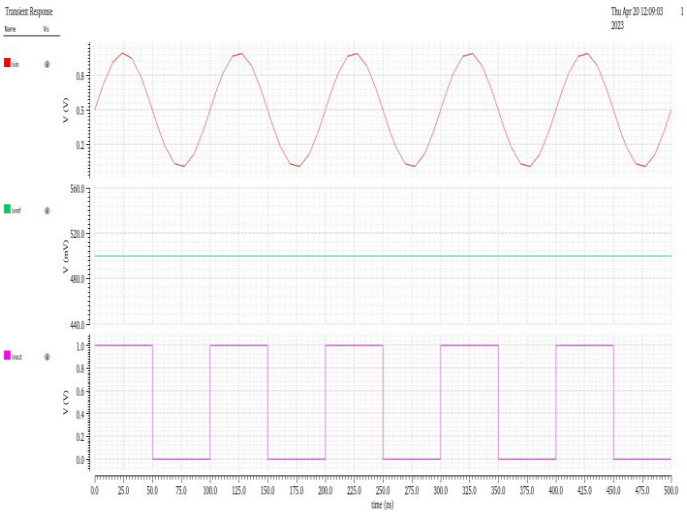

Fig. 7: Transient Response of Comparator Circuit

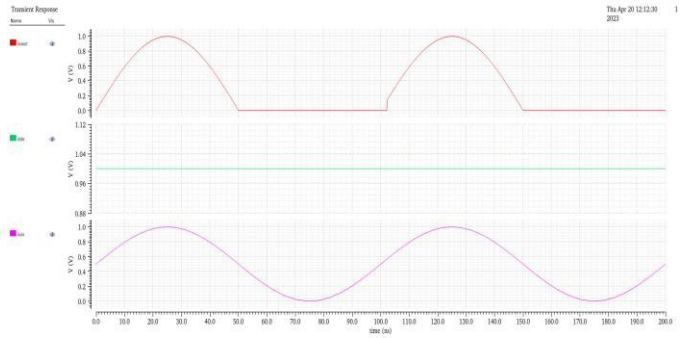

Fig. 8: Transient Response of MDAC for positive cycle

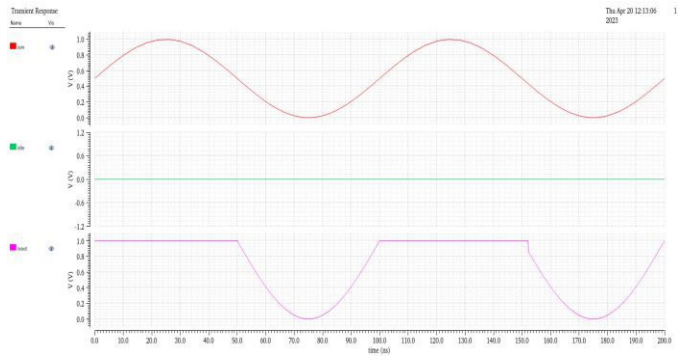

Fig. 9 Transient Response of MDAC for negative cycle

Successive Approximation Register (SAR). Upon the first transition of the clock pulse from low to high, the Most Significant Bit (MSB) of the SAR output, B7, is set to one.

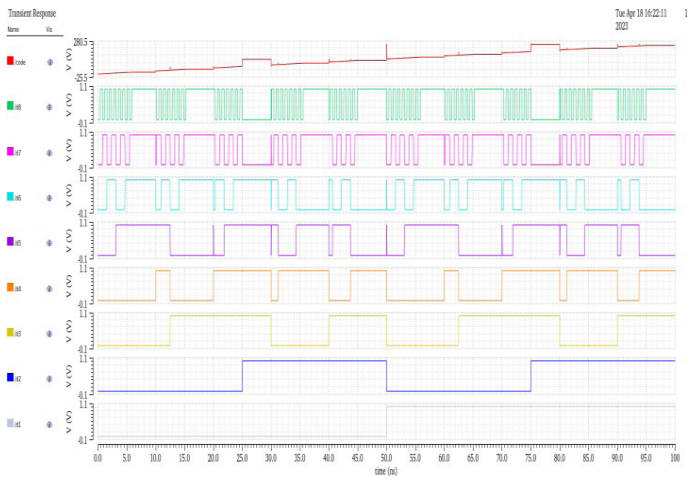

Fig. 10: Response of the SAR control logic

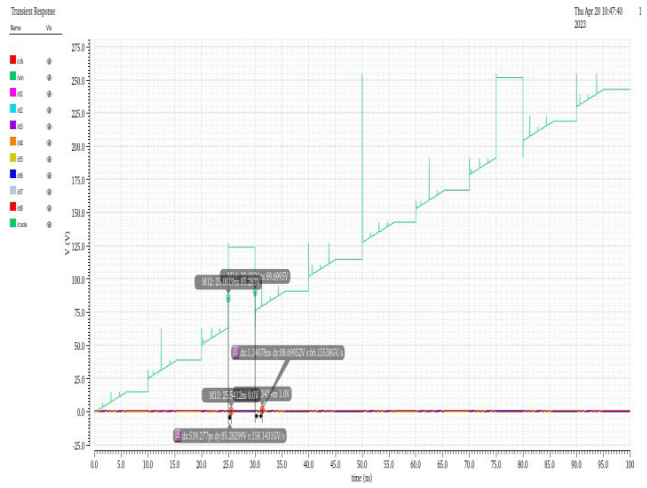

Fig. 11: Delay Response

Table I. Comparison of Different Parameters of Some Papers with this work

Reference	[2]	[5]	[3]	[4]	[8]	[6]	This Work	This Work
CMOS Process	180nm	90nm	0.13um	65nm	90nm	90nm	90nm	180nm
No. of Bits	12	10	10	10	8	8	8	8
Input Supply	1.8v	0.8v	0.8v	1.2v	1.2v	1.3v	0.8v	5v
Speed	1Gsa/s	80Msa/s	60Msa/s	100Msa/s	300Msa/s	30Msa/s	50Msa/s	1Gsa/s

The Digital-to-Analog (D/A) converter then produces an analog equivalent of B7, which is compared to the analog input, vi(0.8). If the comparator output is low, indicating that the D/A output is greater than vi, the SAR will clear and the MSB, B7, will be set. This process is repeated with each subsequent clock pulse transition, setting the next MSB until all bits have been tried, including the Least Significant Bit (LSB), B0. Once the SAR has tried all bits, the result is indicated. In total, it takes 8 clock pulses to complete the analog signal conversion process.

The figures generated through simulation demonstrate that the ADC (analog-to-digital converter) implemented in this study exhibited good performance, yielding satisfactory results. Table I presents a comparison between the findings of this study and those of prior research.

CONCLUSION

The design of an 8-bit successive approximation ADC that can be used for biomedical applications including pacemakers, MRIs, and EEGs is shown in this work. For 180nm CMOS technology, the ADC requires a supply voltage of 5V, while it only requires 0.8V for 90nm CMOS technology. Since the comparator uses more power than the other components of the SAR ADC, the design was focused on creating a low power comparator and Digital to Analogue Converter (DAC). Verilog was used to create the asynchronous SAR control logic. The ADC's total speed was found to be 50Msa/s for 90nm Technology and 1Gsa/s for 180nm Technology, with a sampling rate of 20Msa/s. The S/H circuit required nearly little power.

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