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Detection of Soft Errors in Clock Synthesizers and Latency Reduction Throgh Voltage Scaling Mechanism

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Abstract

In the emerging growth of digital systems, the role of developing self-repairing circuits are demandable. Error tolerance is highly important for such automated platforms to perform well. The heart of any digital system rely on the clock signals opted for overall operation and synchronization. Soft errors in clock signal are serious issues. The proposed work considers the challenges of soft error occurrences in digital circuits such as radiation impact, latency errors, and employ the dual voltage scaling mechanism. The CMOS Schmitt trigger is initially developed with that an voltage scaling mechanism is created. The inputs voltage is varied using the voltage sweep circuit. For a frequency of 5MHz to 5 GHz is considered as the sweep frequency. The step size of sweep frequency is 500KHz. The parameters such as drain voltage (Vd), Source voltage (Vs) are controlled during the process and Gate-Source capacitance and Gate-Drain capacitance is measured. For the sweep frequency the stable clock outputs are generated from the proposed clock synthesizer (CS). The reduction of 0.018 ns of delay latency is achieved at 5GHz input.

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Introduction

Soft errors represent a critical and continuous test for both present and impending registering frameworks. These blunders eminently disintegrate the unwavering quality of the frameworks, prompting possible glitches and information defilement. It is basic to address these soft errors; in any case, the ongoing systems accessible are not developed without their disadvantages. A few existing methodologies bring about unrealistic degrees of region and power utilization above, while others degraded in really in terms of securing situations where various memory cells are impacted at the same time. Soft errors in memory devices are often caused by ionizing radiation, which can be generated by sources such as cosmic rays or radioactive materials. When a high-energy particle interacts with the silicon substrate of a memory cell, it can release charge carriers (electron-hole pairs). These charge carriers can then interfere with the normal behavior of the memory cell, potentially flipping the stored data bit from a 0 to a 1 or vice versa.[1] Redundant storage elements are used to store duplicate copies of critical data. Periodically, data is checked against its redundant copy, and if an error is detected, the correct data is rewritten. Introducing an innovative approach, this study suggests a novel technique for the selection of test vectors in a soft-decision low-complexity Chase algorithm. Unlike conventional methods that demand the computation of multiple polynomials of location or extensive root searches, the proposed technique offers a significant advancement. It enables the pre-selection of decodable test vectors by leveraging solely the syndrome information. Notably, this is achieved with minimal utilization of hardware resources, standing in stark contrast to the resource demands of hard-decision TEC and QEC methods. This advancement not only streamlines the decoding process but also underscores the efficiency of the proposed algorithm in optimizing both computation and resource allocation.[2] The primary strategy revolves around elevating the soft decision Channel Bit Error Rate (CBER) by employing asymmetric Log-Likelihood Ratios (LLRs). This approach harmonizes the distribution of LLRs with that of hard breakdown errors induced by resets. Concurrently, the Reset Correcting Redundancy Flag (RCRF) technique guarantees the rectification of at least one reset-induced error in

every array subsection. Consequently, both the hard and soft decision CBERs witness a notable improvement. It's worth highlighting that the most favorable results materialize when these two approaches are harmoniously integrated, exemplifying a comprehensive performance enhancement.[3] The method that has been introduced demonstrates its effectiveness in dealing with errors that stem from the converters. It achieves a remarkable 100% correction rate for such errors by harnessing diversity redundancy techniques. Additionally, the study's results bring to light the susceptibility of the system's processing unit to potential hangs. However, this vulnerability can be efficiently alleviated by the implementation of watchdog techniques.[4] Further in existing studies, outlines a real-time error detection approach tailored for nonlinear control systems. The objective is to identify sensor and actuator deteriorations, along with malfunctions stemming from soft errors during the execution of control algorithms on digital processors. The method centers on establishing a redundant check state that is intelligently computed. This computation draws from both the present system states and a historical record of previously observed state values and inputs.[5] A comprehensive solution is introduced, incorporating an error recovery assistant logic alongside an in-situ transition detector. This combined approach is meticulously designed to efficiently counter the impact of radiation-induced single- and double-node upsets.[6]

- The proposed study considers various existing challenges such as on soft error occurrence in digital circuits and evaluated a dual voltage scaling mechanism (VSM).
- The VSM enabled clock synthesizer circuit is developed here with the scope of CMOS Schmitt trigger with cascading principle. The input voltage is getting swept and intermediate voltage scaling process takes place.

The rest of the paper is formulated as literature study in Section 2. Challenges and reason behind system tool selection in Section 3. Followed with Design methodology, results and graphs obtained from the proposed tool etc. in section 4 and 5. The results are discussed and concluded in Section 6.

Literature Survey

M.S.M.Siddiqui et al. (2020) as transistors continue to shrink in size, their heightened sensitivity to ionizing radiation effects becomes more apparent. Cosmic rays and other high-energy particles can easily impact these smaller transistors. When these particles collide with a vulnerable node within a semiconductor device, they initiate the creation of electron-hole pairs, which subsequently triggers temporary voltage fluctuations. In memory devices, this phenomenon can induce a bit flip, resulting in what is known as a Single Event Upset (SEU).

K. Naveed et al. (2020) Soft errors pose a significant and ongoing challenge for both present and upcoming computing systems. These errors notably erode the reliability of the systems, leading to potential malfunctions and data corruption. Addressing these soft errors is imperative; however, the current solutions available are not without their drawbacks. Some existing approaches result in impractical levels of area and power consumption overhead, while others fall short in effectively safeguarding against scenarios where multiple memory cells are affected simultaneously. In terms of reducing the time overhead soft error issues are here treated with multi-bit processing enabled Aster approach that reduce the overhead by 5%.

C. Tan et al. (2021) as transistor scaling persists, the susceptibility of soft errors within combinational circuits becomes more pronounced. To address this mounting issue, the industry adopts strategies like Triple Modular Redundancy (TMR) and Gate-Sizing (GS) to bolster the robustness of these circuits. Yet, the conventional TMR approach often applies at the module level, leading to a considerable expansion in the circuit's footprint. The hybrid method reduces the overhead and improves the performance through optimization.

X. Yang et al. (2022) a residual convolutional neural network is developed to denoise the bit stream errors occurring in the channel decoding process. The system clearly depicts the over fading problem comparatively and their by achieving the better reliability on soft error computing systems. the innovative approach aims to achieve a dual objective: the reduction of noise power while simultaneously maintaining the Gaussian distribution of residual noises.

C. -H. Chung et al. (2019) Soft errors arise due to a variety of radiations emitted by silicon chips. In this context, a resistance-based model is embraced to enhance the resilience of IoT systems against these soft errors. Additionally, predictive analyses are carried out to assess the vulnerability of devices to soft errors stemming from line-type multiple-cell upsets (MCUs) under varying radiation conditions. Following this, a comprehensive investigation is conducted using simulations to delve into the characteristics of secondary ions generated by terrestrial neutrons within silicon devices.

N. Pande et al. (2020) Unveiling a wide array of circuit parameters that influence the vulnerability of standard

combinational logic to soft errors in advanced CMOS nodes, a comprehensive study is conducted. A specialized high-density array-based soft-error characterization platform is introduced, encompassing standard logic gate chains of differing lengths. Neutron irradiation data gathered from gate variations utilizing devices with varying channel widths and threshold voltage characteristics is thoroughly examined. This analysis spans multiple supply voltage levels, ranging from nominal values to those approaching near-threshold conditions.

D. Y et al. (2020) the author presented a system exploring on soft error occurrences in d type flip flops. Radiation-hardened benchmark circuits are synthesized using Data-Aware Dual-Rail Flip-Flop cells. These circuits are subsequently employed to validate the efficacy of proposed flip flop cells in mitigating the impact of soft errors, in comparison to a previously established technique known as built-in soft-error resilience (BISER). Remarkably, the utilization of proposed flip flop cells yields a significant 18% reduction in circuit area and a noteworthy 40% enhancement in timing performance when contrasted with the BISER method. In summary, the comprehensive development of proposed flip flop spans from device-level modeling to system-level validation, clearly demonstrating its robust resistance to the effects of soft errors.

On studying various existing frameworks on soft error reduction technique, the factors influencing the soft error generation in in digital systems are formulated below,

- As the increase in voltage fluctuations in semiconductor devices generates subsequent triggers which in turn impact the bit stream errors.
- The major challenge of soft errors included with the potential malfunction of systems. Memory cell is get corrupted due to uncertain occurrence of bit streams.
- The peculiar impact of soft errors in combinational circuits are important, as the transistor scaling happens frequently, the results may impact in combinational circuits also. The impact of soft errors in signals, fluctuations due to radiations are recent problems in digital systems.

Keeping these challenges in digital circuits as serious problem, the presented system considers a benchmark circuit development and keen analysis on parametric level. The proposed system model considers the parameters variations impacted the reduction rate of soft errors through distributed clock synthesizer as test circuit that sweeps various levels of clock frequencies. Various existing soft error tolerant circuits are studied from existing state of art articles [14]-[20].

System Design

The proposed system considers the benchmark circuit development using Distributed clock synthesizer using CMOS circuits, employed with dual scaling transistor for adopting the input voltage. The layout model is initiated with the analog design using Micro wind Tool and supportive code on Verilog. The Verilog code is simulated using ModelSim software in which the Schmitt trigger based circuit is developed with tunable voltage selection module. The inverted output and trigger outputs are monitored without scaling process. Then with the application of voltage tuning process, the results of clock generator and its equivalent voltage vs. Current characteristics are monitored.

Absolutely, the parametric analysis feature within Microwind serves as a potent tool for swiftly exploring the impact of parameter variations on circuit behavior. This functionality accelerates the investigation process, allowing for efficient assessment of how changes in specific parameters influence circuit performance. For instance, the influence of load capacitance on gate delay serves as an illustrative example. By employing the parametric analyzer, the tool autonomously increments the capacitance, conducts a series of simulations, and subsequently presents the results in a comprehensible visual format on the display. This approach streamlines the analysis process, aiding engineers and designers in understanding the intricate relationships between parameters and circuit outcomes.

Methodology

Fig 1. Shows the proposed VSM enabled Clock synthesizer (CS) circuit using Schmitt trigger (ST). The CMOS ST is developed with Pmos and Nmos transistor. Indeed, cascading two Schmitt trigger circuits while utilizing an input voltage as a sweep voltage allows for a controlled variation within a specific range. This arrangement enables the manipulation of the output states based on the input voltage's transition, offering a versatile and precisely adjustable signal processing setup. Two distinct scaling mechanisms have been devised: the first caters to voltage scaling, while the second addresses the intermediate input voltage scaling process. This dual approach allows for a comprehensive and tailored adjustment of voltage levels, enhancing the adaptability and efficiency of the system. The input voltage undergoes a sweeping process with a frequency

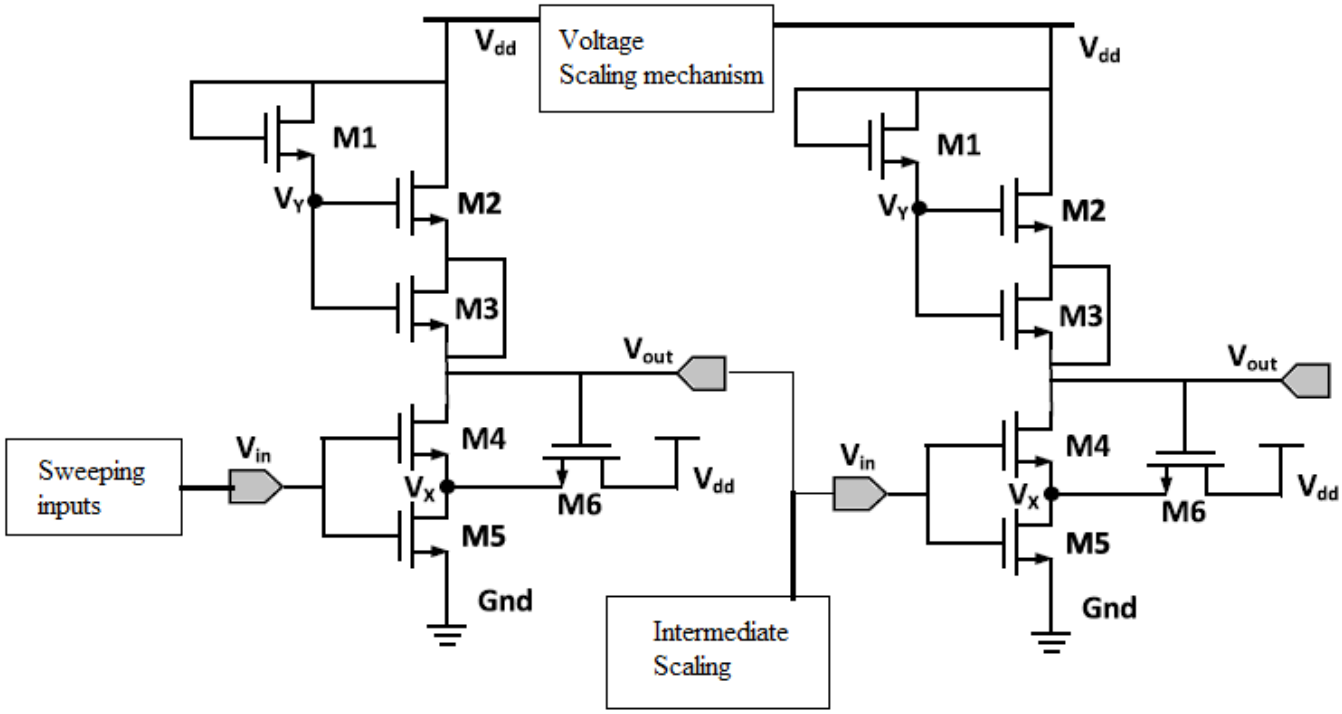

Fig. 1: Proposed VSM enabled Clock synthesizer using Static Schmitt trigger

range spanning from 5 MHz to 5 GHz. This dynamic range of frequency variation introduces a wide spectrum of possibilities for signal analysis and manipulation across various applications. In accordance with the circuit configuration, the Schmitt trigger generates square pulses within a range similar to that of the input frequency. Additionally, the noise inherent in the output pulse is finely tuned by manipulating the voltage scaling mechanism. This strategic adjustment not only ensures synchronization with the input range but also facilitates the optimization of noise levels for enhanced signal quality. As the square wave generation process takes place, the intermediate voltage tuning mechanism dynamically adjusts itself to minimize the occurrence of soft errors in the clock signals. This proactive approach to error reduction contributes to a more robust and reliable operation.

Moreover, an in-depth analysis of the overall latency is conducted in relation to the frequency. This investigation sheds light on how different frequencies impact the system's response time, offering insights for optimization. Furthermore, the capacitance values within the system are deliberately varied, considering the voltages at both the gate (Vg) and drain (Vd) terminals. This meticulous adjustment ensures that the capacitance levels are in harmony with the voltage conditions, enabling fine-tuning of performance parameters to achieve desired outcomes.

Results and Discussions

Table 1: Design overview

NMOS		PMOS	
Width	Length	Width	Length
4	0.2	4	0.2

Table 1. shows the design overview of proposed VSM enabled Clock synthesizer circuit. Here the width of the layout is 4 Micro meter and length is 0.2 Micro meter (um). The standard value of 4, 0.2 is maintained through the design.

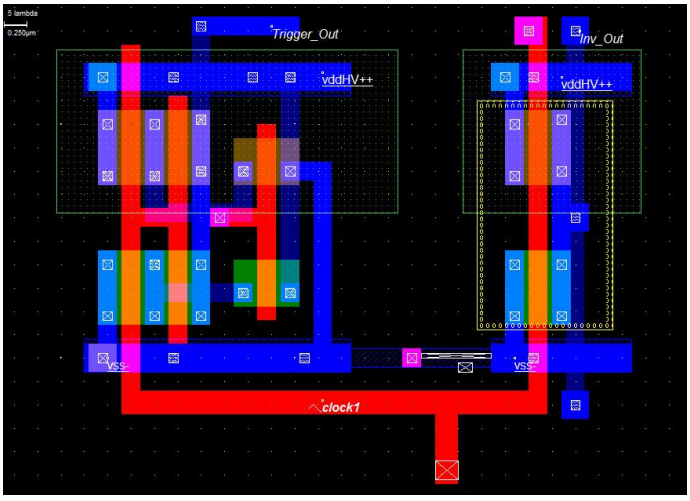

Fig 2. Design view of proposed VSM-CS

Fig 2. Shows the design of VSM-CS model using Microwind tool. The clock outputs are monitored through simulation scope labelled as Trigger. On the other hand trigger outputs are viewed after the scaling process also.

Table 2: Parameters of Proposed VSM-CS

Vd	Vg	Cgs	Cgd
1	1	9.4	1
1.2	1.2	10.4	2
1.4	1.4	10.6	4
1.6	1.6	11	7
1.8	1.8	11.2	8

Table 2. shows the parameters of proposed VSM-CS circuit, by tuning the Vd = 1, 1.2,1.4,1.6,1.8 with Vg = 1,1.2,1.4,1.6,1.8 the equivalent capacitance Cgs and Cgd get tuned.

Fig 3. Shows the tuning process results of Vg, Vd with respect to Cgs, Cgd. As the voltage raises, the charge inside the capacitance get increased.

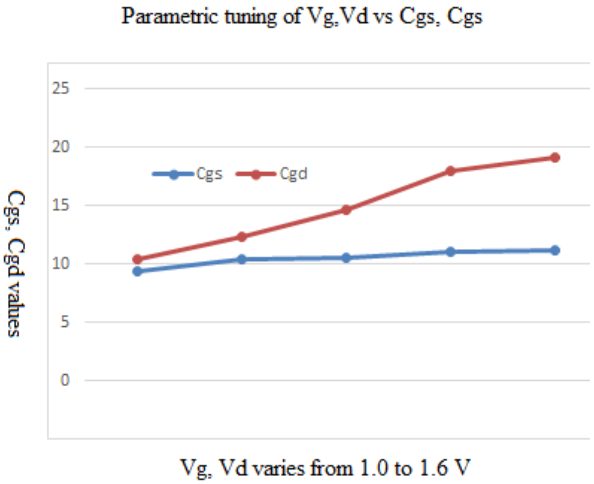

Fig. 3: Parametric tuning process of Vg,Vd Vs. Cgs, Cgd.

Fig 4. Shows the result of NMOS characteristics on high voltage, as the Vd ranges from 0-2.5V and Vg varies from 0 to 2.5 etc. the step size of 0.50 is followed in (Fig 5).

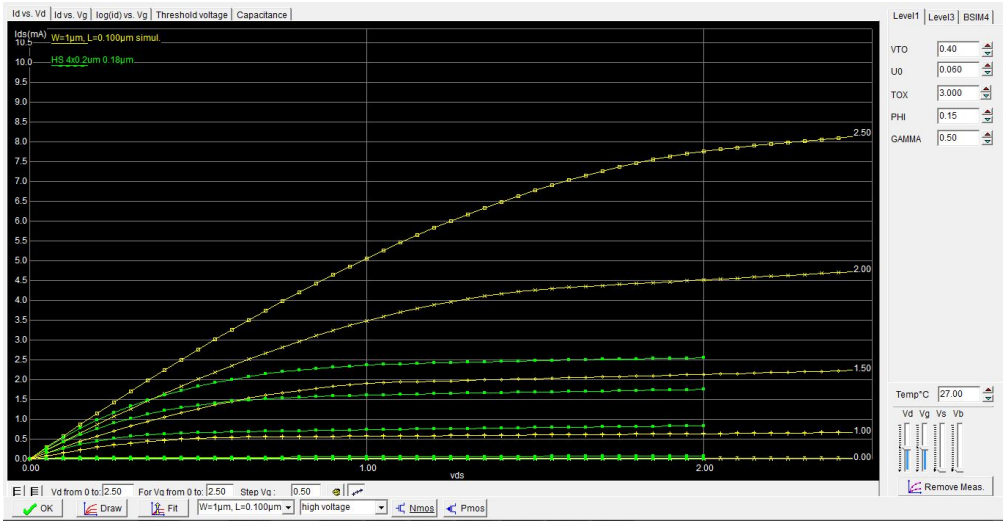

Fig. 4: NMOS performance during High voltage

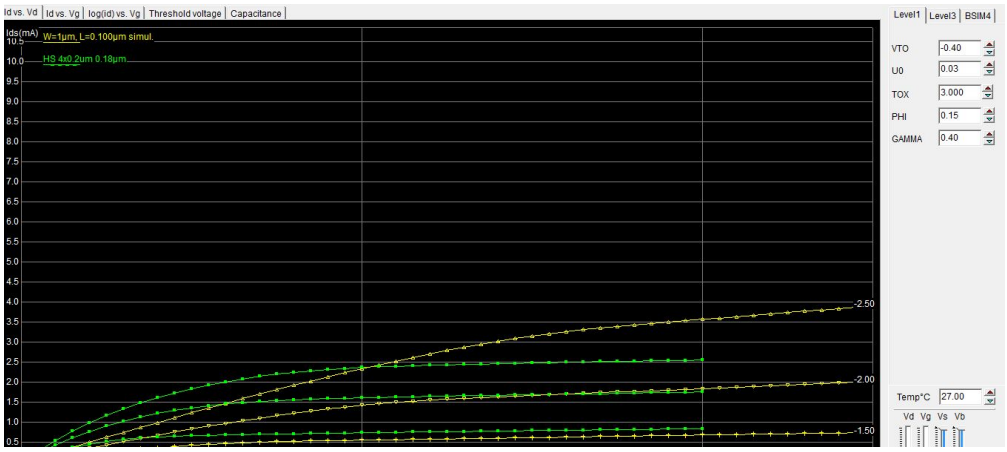

Fig. 5: PMOS performance during High voltage

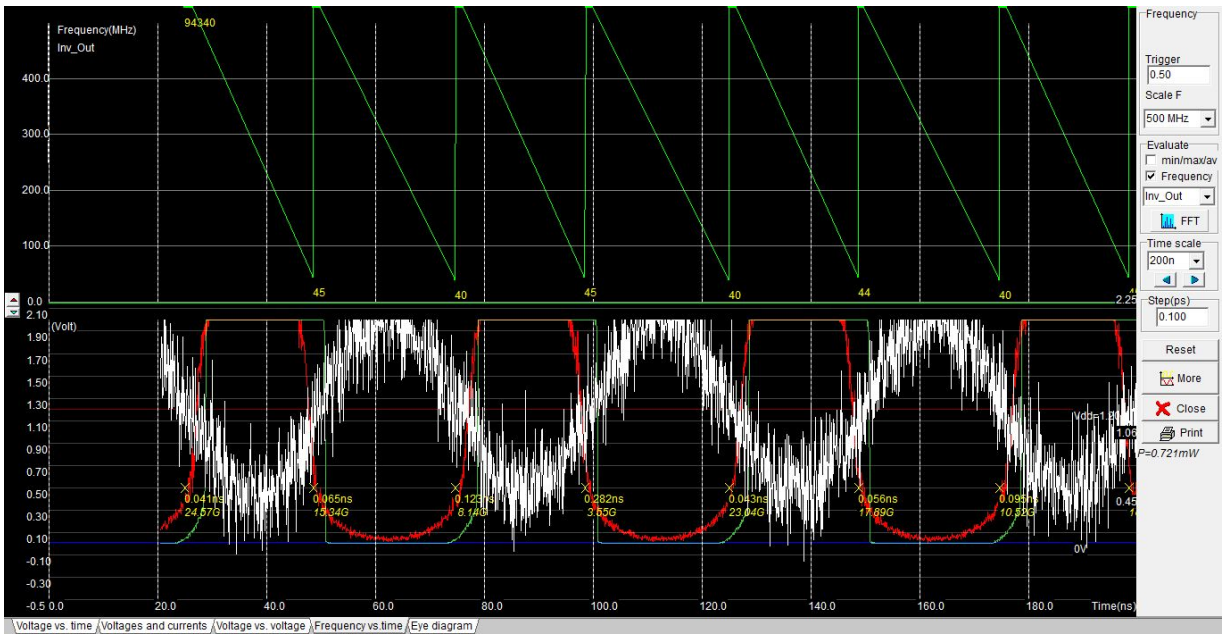

Fig. 6: Result of VSM-CS clock output

Table 3. Performance in terms of Frequency, Power and Latency

Test Count	Frequency	Power in mW	Error latency
1	5	0.723	0.199
2	10	0.722	0.197
3	50	0.721	0.37
4	100	0.726	0.18
5	500	0.721	0.127
6	1000	0.721	0.163
7	2000	0.721	0.211
8	5000	0.720	0.018

Fig 5. Shows the result of PMOS characteristics on high voltage, as the Vd ranges from 0-2.5V and Vg varies from 0 to 2.5 etc. the step size of 0.50 is followed.

Fig 6. Shows the simulation result of VSM-CS clock output as the delay between the triggers are monitored. The detailed error latency reduction values are shown in the Table 3.

Table 3. Shows the power report and error latency of clock pulses with respect to frequency. The frequency range from 5 MHz to 5 GHz. Here the readings

Fig 7. Shows the error latency of proposed VSM-CS model getting reduced during the high frequency switching also. The voltage scaling mechanism plays a crucial role in enabling the Schmitt trigger circuit to adapt flexibly. Its significance extends to the overall process by facilitating the adjustment of latency errors through the systematic application of consistent delays. This dynamic intervention not only enhances the circuit's resilience but also contributes to refining its performance by addressing latency-related challenges.

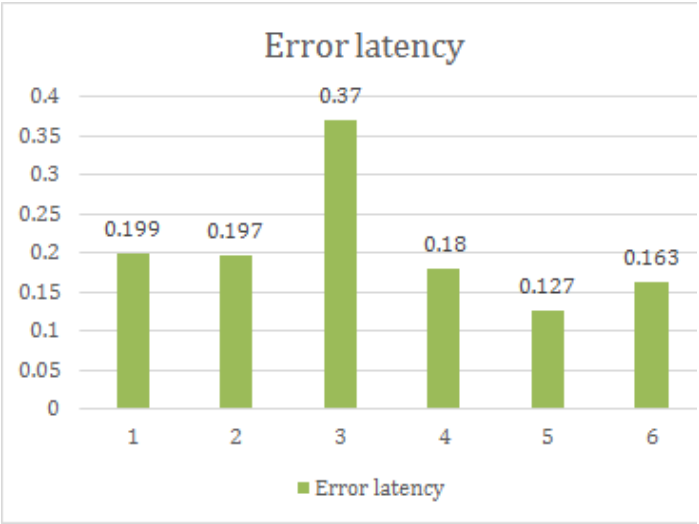

Fig. 7: Error latency

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Conclusion

In the arising development of advanced frameworks, the job of creating self-fixing circuits are demandable. Error resistance is profoundly significant for such mechanized stages to perform well. The core of any advanced framework depend on the clock signals are employed for operational performance and synchronization. Soft errors in clock signal are difficult issues. The proposed work considers the difficulties of soft error events in computerized circuits, for example, radiation influence, dormancy errors, and utilize the double voltage scaling system. The CMOS Schmitt trigger is at first evolved with that a voltage scaling instrument is made. The information sources voltage is shifted utilizing the voltage clear circuit. For a recurrence of 5MHz to 5 GHz is considered as the breadth recurrence. The step size of clear recurrence is 500 KHz. The boundaries like channel voltage (Vd), Source voltage (Versus) are controlled during the interaction and Entryway Source capacitance and Door Channel capacitance is estimated. For the scope recurrence the steady clock yields are created from the proposed clock synthesizer (CS). The decrease of 0.018 ns of postpone inactivity is accomplished at 5GHz information.

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