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Research Article

Analysis of Low power and reliable XOR-XNOR circuit for high Speed Applications

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ABSTRACT
This paper presents a comprehensive study of different types of XOR-XNOR circuits. Our main focus is to characterise the XOR-XNOR combinational circuit design using six transistors for low power applications. The six transistor XOR-XNOR circuit can be simulated using 45nm CMOS technology in cadence virtuoso using foundry files. The simulation results demonstrates, parameters such as power, delay and power delay product(PDP) at different voltages ranging from 0.4 to 1v respectively. From the obtained results it clearly indicates the proposed design has low power consumption and full voltage swing.

Keywords: Low power, XOR-XNOR, power

INTRODUCTION

As the day by day scaling down of the VLSI technology, power and area becomes one of the critical issue in the present day scenario. At present day high speed processors are operating at very high frequencies(GHz), Hence it is necessary to reduce the power consumption, which may improves the reliability of the system. In recent years XOR and XNOR plays a major role in many applications such as adders,compressors,comparators, error detection and correction ,communication ,linear systems and so on[1].The optimized set of XOR-XNOR circuit provides better advantages in terms of noise immunity, low power, less delay, full output voltage swing etc. another advantage of the proposed XOR-XNOR circuit will produces the a generous and non skewed output. The XOR function is a odd function and i.e. Its output is equal to 1 if any one of the input is equal to 1 and on the other hand XNOR function is even function it will produces the output is 1 when the both inputs are equal to 1 or 0.let us take the inputs are A and B. the XOR of A and B denoted by AØB and XNOR can be denoted by A⊙B. The logic symbol of XOR and XNOR circuits as shown in Fig1 and 2 and table:1 can be illustrated by truth table of XOR and XNOR.

Table1:Truth table for XOR-XNOR.

A	B	Y=A(XNOR)B	X=A(XOR)B
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

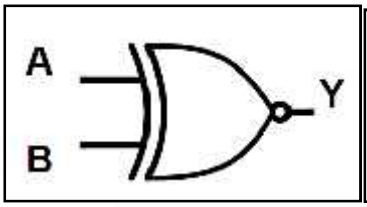

Fig 1:XNOR

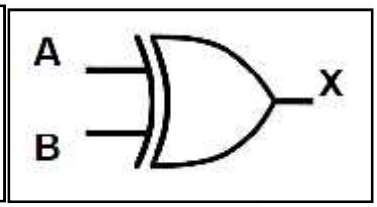

Fig 2:XOR

Previous work

Several designs were proposed to realize the XOR-XNOR functions using different logic styles[2].The first design of the XOR-XNOR circuit implemented by the pass transistor logic[3],which offers the low power consumption but produces the non-full voltage swing and it has limited driving capability. the pass transistor based XOR-XNOR circuit can be depicted by the fig3. respectively.

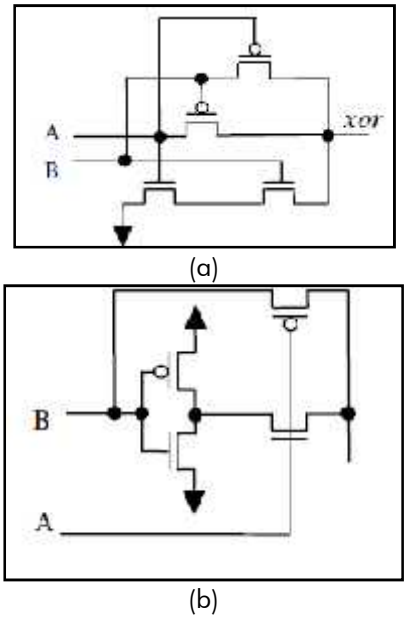

Fig 3: Pass transistor based XOR- XNOR circuits

In order to improves the signal level and to enhances the driving capability proposed a static CMOS inverter with conjunction based MUX[4-5]. The availed inverter enhances the power level of the signal and increases the voltage swing of the XOR and XNOR considerably. The architecture of the power less XOR and grounded XNOR circuits shown by Fig 4and 5 respectively. But These circuits imposes the power level but provides poor propagation delay and vulnerable to environmental variations. and also these designs unable to produce the full voltage swing when scaling down the transistors at deep submicron level.

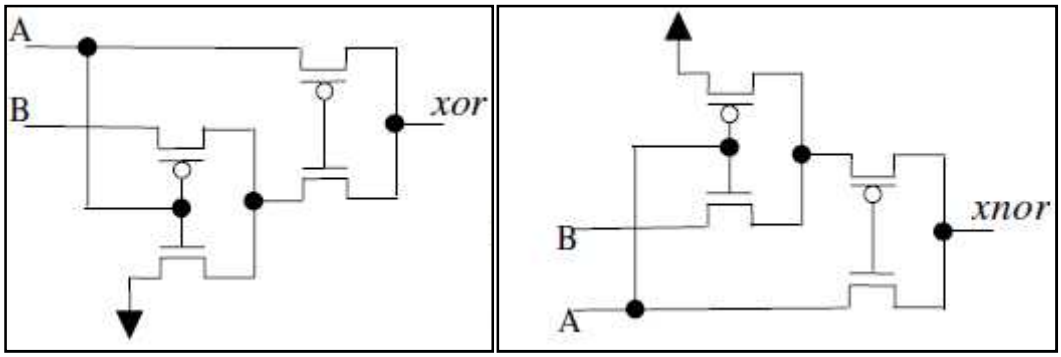

Fig4: Power-less XOR **Fig 5:Ground-less XNOR**

To overcome the above mentioned flaws in the previous design, proposed a static CMOS based XOR-XNOR circuit which increases the power level and noise margin of the circuit. The design is composed of two transmission gates and three static inverters respectively.The static inverters helps to improve the capability of the circuit under dynamic conditions[6-7]. But the circuit can suffers from more power consumption. The circuit diagram of the 10 transistors as shown in fig 6.

XNOR-XOR schematic

To overcome the power consumption and to generate the full swing voltage proposed a 6 transistor XOR-XNOR circuit. The proposed 6 transistor XOR-XNOR circuit utilizes the advantages of the both pass transistor and static inverters. The main motto of the CMOS inverter is used to enhance the full swing at each and every instance of the comination.VDD connection to the transistor M3 and M4 are used to drive the output of '1' and M4 is used to drive the output signal whenever the XOR output is "0",provided input of the A and B are 1. At the scenario M1 and M2 are ON,it propagates output to 1.As XOR produces as output is '0'. Fig 7 depicts the circuit diagram of the 6 transistors respectively.

Simulation Setup

The XOR-XNOR circuit were simulated using cadence spectre ranging from 0.4 to 1v using 45nm CMOS technology. Simulation is carried out from different voltage nodes and estimated the corresponding power dissipation values. this analysis were carried

out for existed XOR-XNOR circuits. The obtained readings were taken at the ambient temperature at 27^0C.The comparison of the XOR-XNOR circuits results for each combination illustrated by the table2.and we have also drawn layout for the circuit(Fig 8) and verified the DRC,LVS and RC extraction. From the obtained results found that the circuit improves the overall PDP more than 50% and similarly it consumes the low power. the final output wave form of the proposed 6 transistor as shown in Fig9.

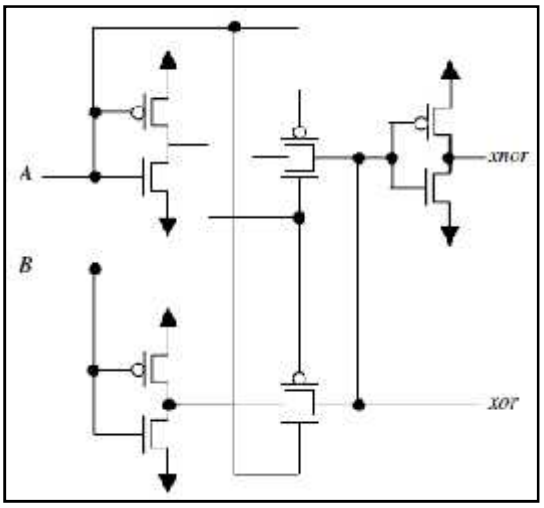

Figure 6. 10 transistor circuit for XOR-XNOR function.

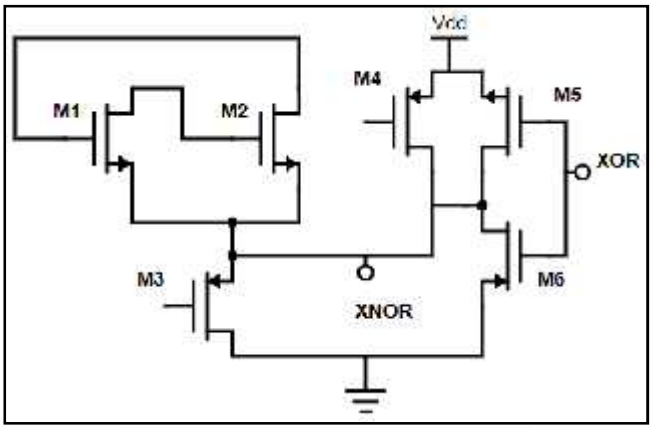

Fig 7: proposed XOR-XNOR circuit

Table 2:Comaprision of different types of XOR-XNOR circuits at different voltages

	Voltage(V)	Proposed(6T)	8T [3]	10T [3]
Delay of XOR(ns)	0.45	3.4526	2.253	4.256
	0.55	2.3625	2.465	3.256
	0.75	2.3562	2.3625	2.365
	1	2.1235	2.0145	2.958
Delay of XNOR(ns)	0.45	3.4526	2.1235	2.356
	0.55	2.3625	3.4526	2.1535
	0.75	2.3562	2.3625	3.4621
	1	2.1235	2.3562	2.3658
Average power of XOR(fW)	0.45	5.235	22.36	45.63
	0.55	10.235	32.25	56.36
	0.75	12.369	41.25	78.36
	1	15.235	52.36	89.36

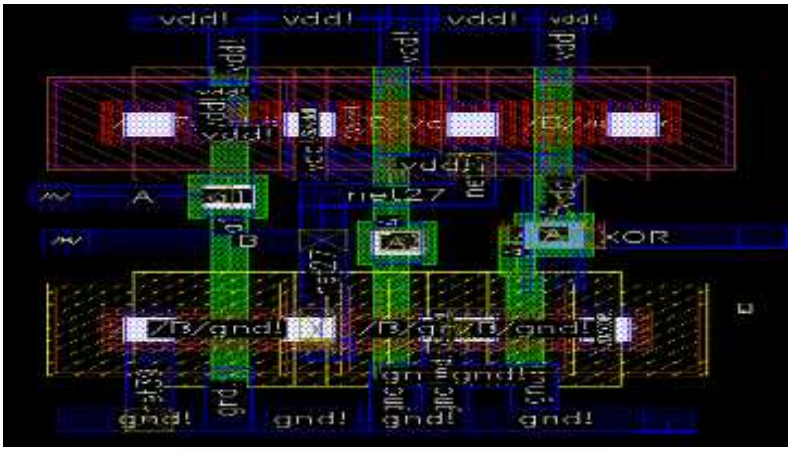

Fig 8: Layout for XOR-XNOR circuit.

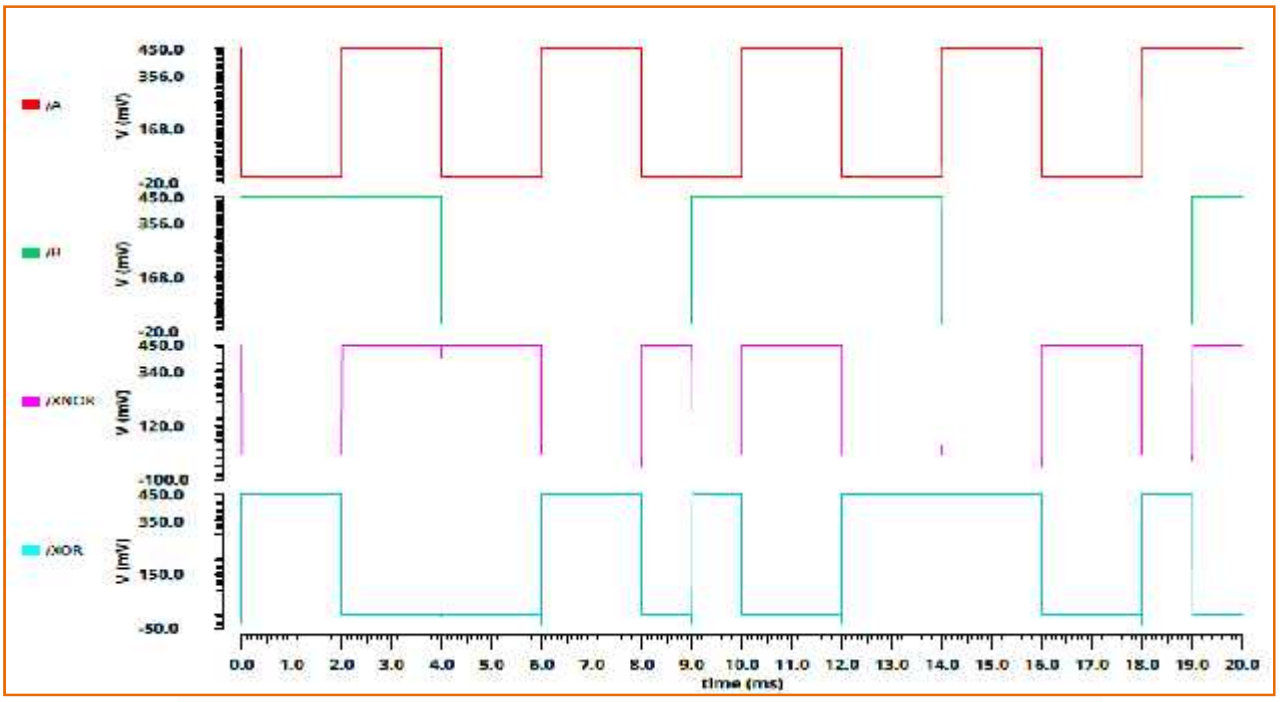

Fig 9: Output wave from for the XOR-XNOR in CMOS 45 nm CMOS technology

Conclusion

In this paper we proposed a novel CMOS XOR-XNOR circuit to enrich the performance of the ALU, comparators, Compressors.etc.This architecture helps to provide the full swing at any stage of the input combination and maintains the better noise immunity. Hence from the obtained results it clearly indicates that the proposed XOR-XNOR circuit widely used for low power and high speed applications.

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